TC7000

(MBA AND TM03/TU77 COMPATIBLE)

TAPE COUPLER

TECHNICAL MANUAL

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TC7551001 Rev E
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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions in this technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The information in this manual is for informational purposes and is subject to change without notice.

Emulex Corporation assumes no responsibility for any error which may appear in this manual.

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EMULEX PRODUCT WARRANTY

TAPE COUPLER/CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex tape controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adapters, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product in such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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Section 1
GENERAL DESCRIPTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the TC7000 Tape Transport Coupler manufactured by Emulex Corporation. In addition, this manual provides diagnostics and application information.

The contents of the eight sections and two appendices in this manual are briefly outlined in the following descriptions:

Section 1 **General Description:** This section contains an overview of the TC7000 Tape Transport Coupler and describes features, compatibility, and performance.

Section 2 **Specifications:** This section presents electrical and physical specifications for design parameters in tabular form for easy reference.

Section 3 **Applications and Configuration:** This section describes configuration of applications to help the user choose bus addresses, interrupt vector addresses, and mapping of logical/physical disk drives for optimum system performance.

Section 4 **Installation:** This section contains the information necessary to set-up and physically install the TC7000 Tape Coupler.

Section 5 **Troubleshooting:** This section describes fault isolation procedures that can be used to pinpoint trouble spots.

Section 6 **Registers, Commands and Programming:** This section contains descriptions of words, fields, bytes, and bits in all tape coupler registers, and describes the commands and programming techniques on which the tape coupler register set was developed.

Section 7 **Functional Description:** This section contains a description of tape coupler architecture and formats used on the tape transports to help the programmer write effective programs.

Section 8 **Interfaces:** This section contains pin/signal assignments for the CPU and peripheral interfaces.

Appendix A **TC7000 Tape Coupler Configuration and Option Selection:** This appendix provides instructions for configuring the TC7000 Tape Coupler and for selecting options by means of switches.

Appendix B **Specific Configurations:** This appendix provides instructions for making proper jumper connections and switch settings for various options on specific tape transport models..

This section is divided into five subsections, as listed in the following table:

Subsection	Title
1.1	Scope
1.2	Overview
1.3	Physical Description
1.4	Features
1.5	Compatibility

1.2 OVERVIEW

The TC7000 Tape Coupler is a single extended hex-sized printed circuit board assembly (PCBA) which can be plugged directly into connectors A, B, and C of slot seven, eight, or nine of a Digital Equipment Corporation (DEC) VAX-11/750 central processing unit (CPU) backplane, or which can become a component of an Emulex V-MASTER/780 card cage unit.

Embedded as a single PCBA in the VAX-11/750 CPU, the TC7000 Tape Coupler provides a CPU Memory Interface (CMI) to interconnect with the CPU and L0016 Memory Controller.

The V-MASTER/780 is a unique new approach for interfacing mass-storage peripherals to the DEC VAX-11/780 CPU. The V-MASTER/780 consists of two Synchronous Backplane Interface (SBI) PCBAs and up to two Emulex Tape Couplers or Disk Controllers (TC7000 or SC7000, respectively) in a compact, four-slot card cage which is installed directly in the VAX-11/780 CPU cabinet. The interface between the V-MASTER/780 and the TC7000 Tape Coupler is called the V-MASTER Memory Interface (VMI) bus which is electrically, but not logically, identical to the CMI. The interface between the V-MASTER/780 and the VAX-11/780 CPU is the SBI bus.

The TC7000 Tape Coupler includes an associated Cable Paddleboard PCBA that provides connectors for tape transport interfacing.

The TC7000 Tape Coupler emulates the DEC model TM03/TU77 Massbus tape subsystem, including the DEC RH750 and RH780 MBAs and the logic in each of up to eight tape transports connected to the Massbus. The TC7000 Tape Coupler is able to operate with tape

transports that have different characteristics than those used in DEC subsystems. The variety of tape transports subsystems that can be supported by the TC7000 Tape Coupler is enabled by simple changes in configuration selections made in dual in-line package (DIP) switch settings.

The TC7000 Tape Coupler is hardware compatible with Pertec, or Storage Technology Corporation (STC), or equivalent formatted tape transport systems.

NOTE

> The TC7000 Tape Coupler never interfaces directly with the tape transports, but with the formatter for the tape transports, so tape speed and density are both irrelevant to the TC7000 Tape Coupler. System tape transports can operate at any tape speed up up to 200 inches per second (ips) and with the nine-track non-return to zero inverted (NRZI) format at 800 characters per inch (cpi), or in phase encoded (PE) format at 1600 or 3200 cpi, or in group code recording (GCR) format at 6250 cpi. The TC7000 Tape Coupler is software compatible with DEC TM03 formatter and TU77 tape transport subsystems.

The CPU interface is a tri-state CMI (or VMI) bus that is 32 bits wide. The interface between the TC7000 Tape Coupler and the tape transports consists of two or four cables attached to an associated paddleboard PCBA. The TC7000 Tape Coupler can interface with up to eight Pertec or up to four STC tape transports by means of these cables. The tape transports may be certain combinations of nine-track NRZI, PE, GCR, dual-density (NRZI/PE or PE/GCR), or tri-density (NRZI/PE/GCR) with any mix of tape speeds. Density combinations allowed in the system depend on selection possibilities allowed by the configuration switches (see appendices). A typical tape transport subsystem arrangement for the TC7000 Tape Coupler is diagrammed in Figure 1-1.

1.3 PHYSICAL DESCRIPTION

The TC7000 Tape Coupler PCBA, the Cable Paddleboard PCBA, the Bus Interface PCBA, and the Bus Translator PCBA are shown in Figure 1-2. In the VAX-11/750 CPU system, only the TC7000 Tape Coupler PCBA and the Cable Paddleboard PCBA are required.

The TC7000 Tape Coupler is constructed as one extended hex size PCBA that plugs directly into connectors A, B, and C of Massbus controller slot seven, eight, or nine in the VAX-11/750 backplane or in slot three or four in the V-MASTER/780 card cage backplane. The male side of the CPU or V-MASTER/780 backplane slot in which the TC7000 Tape Coupler is installed connects to a Cable Paddleboard PCBA that is used to provide the interface cable

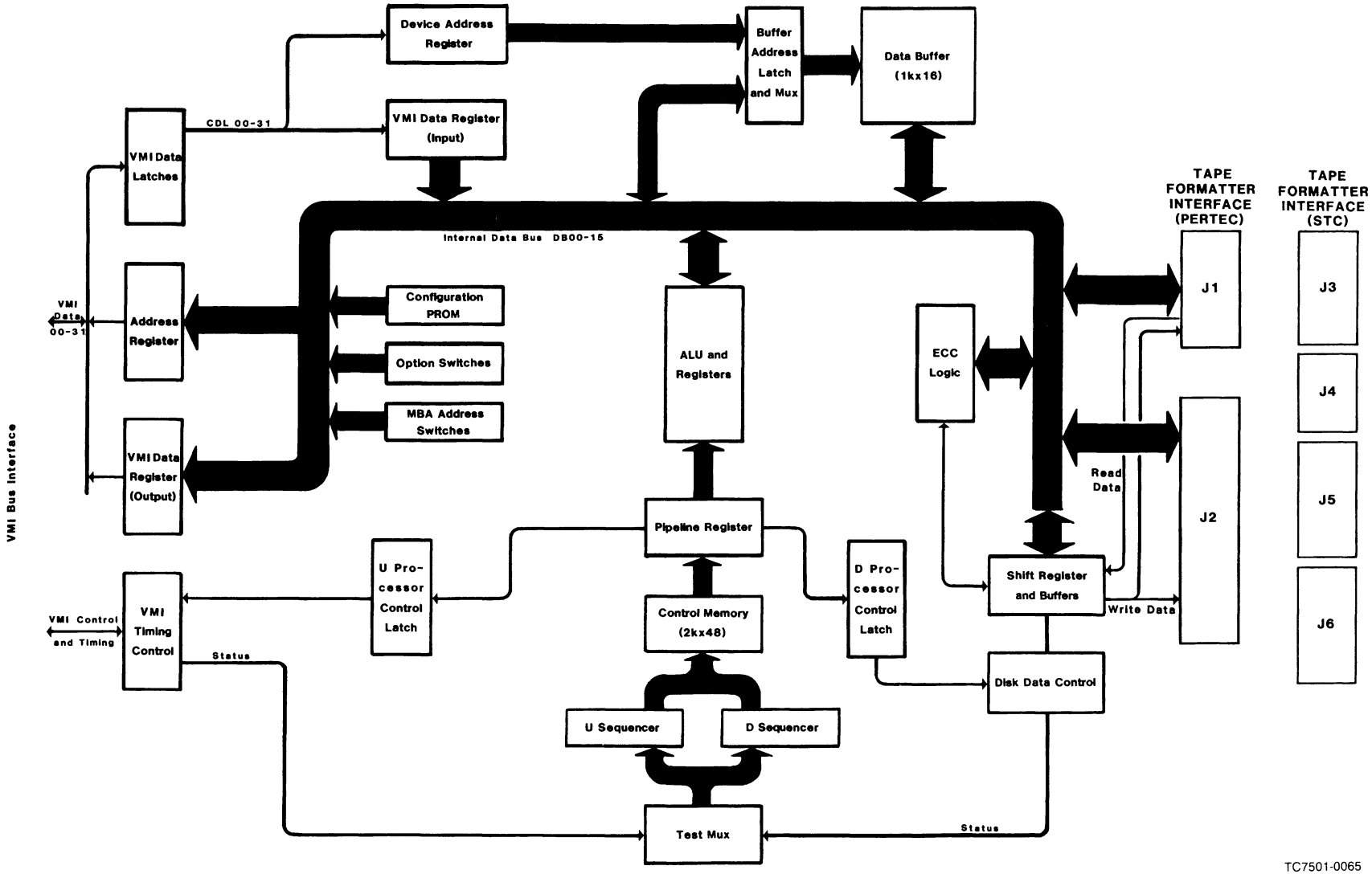

Figure 1-1. TC7000 Tape Coupler System, Block Diagram

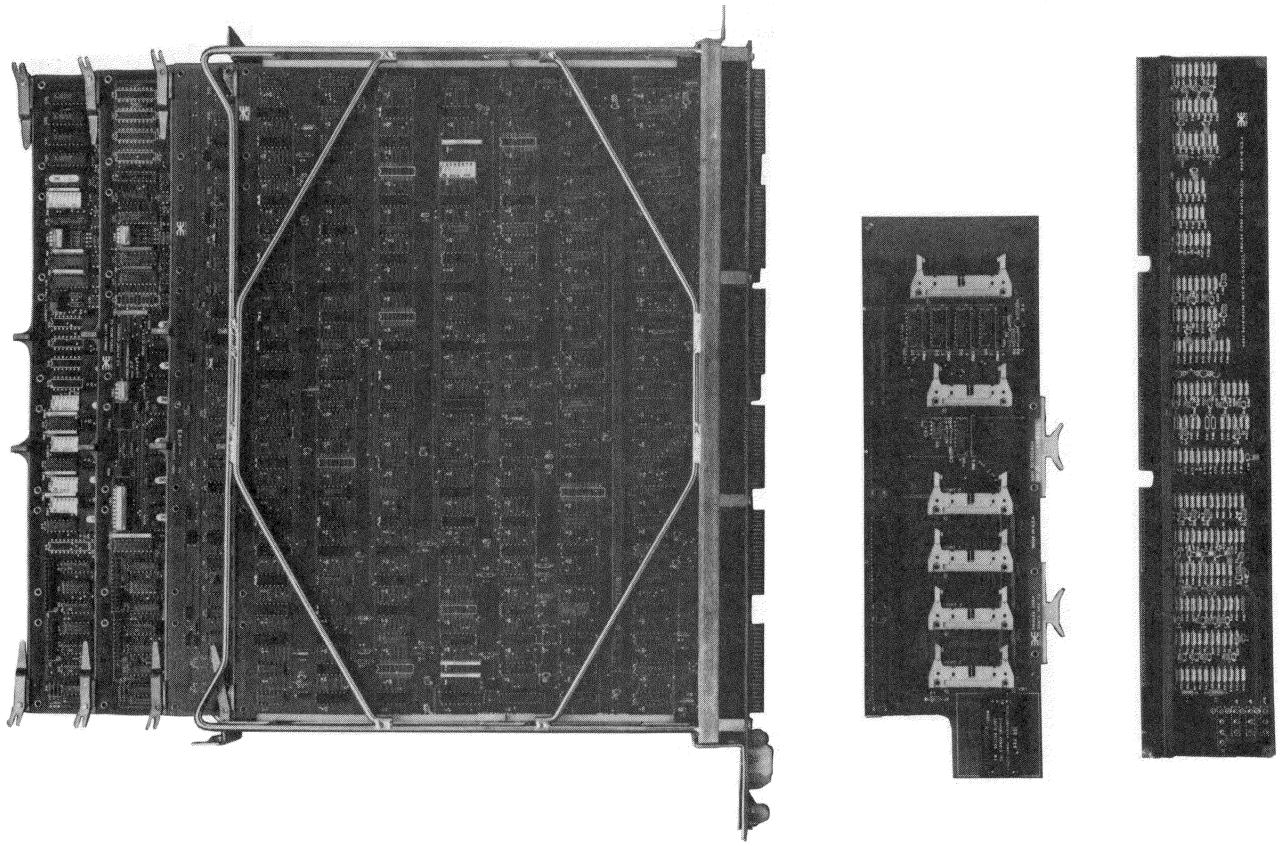

Figure 1-2. TC7000 Tape Transport Coupler System PCBAs

connectors that connect the TC7000 Tape Coupler with the formatter for the system tape transports. The Cable Paddleboard PCBA has six connectors. Connectors J1 and J2 interface (via cables) with the formatter for the first Pertec tape transport. Connectors J3 through J6 interface (via cables) with the formatter for the first STC tape transport. The system cannot mix Pertec and STC tape transports.

1.3.1 V-MASTER/780 ASSEMBLY

The V-MASTER/780 assembly consists of a four-slot, wire-frame, card cage with an integral backplane and the Bus Interface and Bus Translator PCBAs in slots one and two, respectively. Slots three and four can each accommodate one TC7000 Tape Coupler PCBA or one SC7000 Disk Controller PCBA (one Cable Paddleboard PCBA is required for each TC7000 Tape Coupler or SC7000 Disk Controller PCBA). The card cage is designed to mount in the DEC VAX-11/780 CPU chassis in place of the DEC RH780 MBA or the SBI terminator. Card cage dimensions are 3.125 x 20 x 13.375 inches.

1.4 FEATURES

The TC7000 Tape Coupler design incorporates several features that enhance usefulness, serviceability, and performance. Emulex tape controllers/couplers achieve performance that excels the performance of DEC controllers and MBAs, which they emulate, by providing enhancement features such as built-in self test during power-up, and built-in optional selection of various densities and tape speeds for tape transports which are not available on the DEC TM03/TU77 system.

1.4.1 MICROPROCESSOR ARCHITECTURE

The TC7000 Tape Coupler circuitry includes a unique 16-bit, bipolar microprocessor that performs all controller functions. The microprocessor design approach provides a reduced component count, high reliability, easy maintainability, and the means to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The microprocessor is constructed from AMD 2901 bit-slice components. Execution time for microinstructions varies in accordance with CPU operation because the clock for the TC7000 Tape Coupler is tied to the system clock. The Emulex tape couplers achieve functional capability beyond that of the DEC controllers or MBAs which they emulate, by providing enhancement features such as built-in self-test during power-up, and the ability to work with tape transports of various tape speeds and densities. The TC7000 Tape Coupler can handle data transfer rates of up to 1.5 megabytes/second.

1.4.2 PACKAGING

The TC7000 Tape Coupler is constructed as a single, extended, hex-sized multiple-layer PCBA (Emulex P/N TU7510401). No cabling is

required between the CMI Bus on the CPU backplane, or between the VMI Bus on the V-MASTER/780 backplane, and the TC7000 Tape Coupler because the TC7000 Tape Coupler plugs directly into that backplane. The TC7000 Tape Coupler obtains its power from the CPU and no external power source is required.

1.4.3 SELF TEST

The TC7000 Tape Coupler firmware incorporates an internal self-test routine which is executed when the computer/tape transport system is powered up. This test exercises all parts of the microprocessor, buffer, and data-handling logic. This test does not completely test all circuitry in the TC7000 Tape Coupler, but successful completion indicates high probability that all circuits in the TC7000 Tape Coupler are operational. If the TC7000 Tape Coupler fails the self-test operation, the FAULT light emitting diode (LED) on the front edge of the TC7000 Tape Coupler PCBA illuminates and the TC7000 Tape Coupler cannot be addressed from the CPU.

1.4.4 BUFFERING

The TC7000 Tape Coupler contains a 1K x 16-bit high-speed random access memory (RAM) buffer that is used to temporarily store the contents of the Massbus Adapter (MBA) Registers, Device Registers, and Map Registers (see Section 6), plus 512 bytes of data.

1.4.5 OPTION AND CONFIGURATION SWITCHES

Five DIP switch packs are used to configure the TC7000 Tape Coupler for various tape speeds, densities, certain firmware options, MBA number, and arbitration level.

1.5 COMPATIBILITY

The TC7000 Tape Coupler is compatible with functionality, media, diagnostics, and operating systems to the extent described in this subsection.

1.5.1 FUNCTIONALITY

The TC7000 Tape Coupler is functionally compatible with the DEC RH750 and RH780 Massbus Adapters with up to eight Pertec or four STC tape transports attached, except the TC7000 Tape Coupler does not execute the diagnostic mode of the RH750 or RH780 MBA (as applicable) or the Maintenance mode of the DEC TU77 tape transport. The absence of the Diagnostic mode prevents running the complete RH750 or RH780 set of diagnostic programs.

1.5.2 TAPE TRANSPORTS

The TC7000 Tape Coupler is compatible with the nine-track Pertec and STC tape transports that can be operated at data densities from 800 cpi (NRZI) up to 6250 cpi (GCR), and at all standard tape

speeds. The TC7000 Tape Coupler can handle tape transport data transfer rates up to 1.5 megabytes/second.

The TC7000 supports read reverse in GCR mode only on tape transports which have this feature built in. If your tape transport does not support read reverse, the TC7000 will not provide it.

1.5.3 DIAGNOSTICS

The TC7000 Tape Coupler executes the standard diagnostics listed in Section 4.

1.5.4 OPERATING SYSTEMS

By emulating the DEC model TM03 Formatter and the associated TU77 tape transport, the TC7000 Tape Coupler is compatible with the VAX/VMS operating system.

Section 2
SPECIFICATIONS

2.1 OVERVIEW

This section contains the general, electrical, and physical specifications for the TC7000 Tape Coupler. This section is divided into four subsections, as listed in the following table:

Subsection	Title
2.1	Overview
2.2	General and Electrical Specifications
2.3	Physical Specifications
2.4	V-MASTER Specifications

2.2 GENERAL AND ELECTRICAL SPECIFICATIONS

General and electrical specifications for the TC7000 Tape Coupler are listed and described in Table 2-1.

Table 2-1. TC7000 Tape Coupler General and Electrical Specifications

Parameter	Description
GENERAL FUNCTIONS	
Emulation	DEC RH750 OR RH780 Massbus Adapter (MBA) and TM03 Tape Formatter with a single TU77 slave tape transport unit per formatter
Media Compatibility	1/2-inch wide magnetic tape per ANSI standard X3.40-1976
Tape Transport Interface	Formatter for Pertec or STC units
Tape Transports Supported	Up to 8 Pertec or up to 4 STC
Data Block Capacity	UP to 65,536 data bytes
Number of Tracks	Per formatter and tape transport limitations
Tape Speed	All standard tape speeds
Density	Per formatter and tape transport limitations

Table 2-1. TC7000 Tape Coupler General and Electrical Specifications (continued)

Parameter	Description
GENERAL FUNCTIONS (cont'd)	
Computer Interface	VAX-11/750: CMI BUS V-MASTER/780: SBI VAX-11/780: VMI Bus
CMI Address (VAX-11/750)	F28000, F2A000, F2C000 and F2E000
SBI Address (VAX-11/780)	20008000 to 20016000
Interrupt Vector Address (VAX-11/750	150, 154, 158 and 15C
Nexus Address (VAX-11/780)	TR3-TR11
Priority Level	BR5 on VAX-11/750, selective from BR4 through BR7 on V-MASTER
Data Buffering	512 bytes
Data Transfer	32-bit DMA via CMI or VMI Bus
Self-Test	Extensive internal self-test on powering up
Indicators	ACTIVITY and FAULT LEDs
ELECTRICAL	
CMI/VMI Bus Interface	DEC approved line drivers and receivers
Tape Transport Interface	Open collector line drivers and TTL receivers. Cable length accumulative to 20 feet.
Power Required	+ 5 Volts direct current (Vdc), 10 Amperes (A) maximum

2.3 PHYSICAL SPECIFICATIONS

Physical specifications for the TC7000 Tape Coupler are listed and described in Table 2-2.

Table 2-2. TC7000 Tape Coupler Physical Specifications

Parameter	Description
PHYSICAL	
Design	High-speed bipolar microprocessor with 2901-type bit-slice components
Packaging	1 DEC extended hex-size TC7000 Tape Coupler PCBA 1 Cable Paddleboard PCBA 1 DEC extended hex-size Bus Interface PCBA (VAX-11/780 only) 1 DEC extended hex-size Bus Translator PCBA (VAX-11/780 only)
Mounting	Any VAX-11/750 Massbus controller slot (slot 7, 8, or 9) V-MASTER/780 slot 3 or 4
Tape Transport Connection	Cable Paddleboard PCBA on rear of CPU or V-MASTER backplane has 2 connectors for interface with Pertec-type tape transports and 4 connectors for interface with STC tape transports

2.4 V-MASTER SPECIFICATIONS

Specifications for the V-MASTER/780 are listed and described in Table 2-3.

Table 2-3. V-MASTER/780 Specifications

Parameter	Description
CARD CAGE	
Type	Wire frame
Slots	4 Slot #1 for Bus Interface PCBA Slot #2 for Bus Translator PCBA Slot #3 for first Controller PCBA Slot #4 for second Controller PCBA
Backplane	SBI
Replaces	DEC RH780 MBA or SBI Terminator Module in VAX-11/780 CPU Backplane
Power Required	DEC or Emulex power supply (see subsection 4.5)
Dimensions	3.125 inches (in.) wide 20 in. high 13.375 in. deep

Section 3
APPLICATIONS AND CONFIGURATION

3.1 OVERVIEW

This section contains information to help plan installation of the TC7000 Tape Coupler subsystem. Using a few minutes to plan the configuration of the subsystem application can result in a smoother installation with less system-down time. As a planning tool, this section describes some practical matters that should be understood before installation begins.

This section includes application examples and configuration procedures, and is divided into five subsections, as listed in the following table:

Subsection	Title
3.1	Overview
3.2	Application Examples
3.3	Configuration Defined
3.4	Configuration Aids
3.5	Optimizing Performance

Using the information in this subsection should ensure optimum performance from the TC7000 Tape Coupler subsystem. A simplified diagram of a typical system hook-up is shown in Figure 3-1.

3.2 APPLICATION EXAMPLES

The TC7000 Tape Coupler is designed to interface with DEC VAX-11/750 and VAX-11/780 CPUs and with up to eight Pertec or four STC formatter/tape transport subsystems.

3.2.1 CMI

The CMI with the VAX-11/750 CPU is an interface established by installing the TC7000 Tape Coupler directly in slot seven, eight or nine (slot nine preferred for easiest installation) of the CPU backplane.

3.2.2 VMI/SBI

The VMI/SBI with the VAX-11/780 CPU is an interface system established by installing the TC7000 Tape Coupler in a V-MASTER/780 card cage assembly, then installing the V-MASTER in MBA slot one of the VAX-11/780 CPU, or in the Bus Terminator slot of the CPU, or in a DEC expansion box. The V-MASTER provides an SBI-type interface with the VMI so that quad words may be made from dual words, and vice versa. The VMI is electrically, but not logically, identical to the CMI.

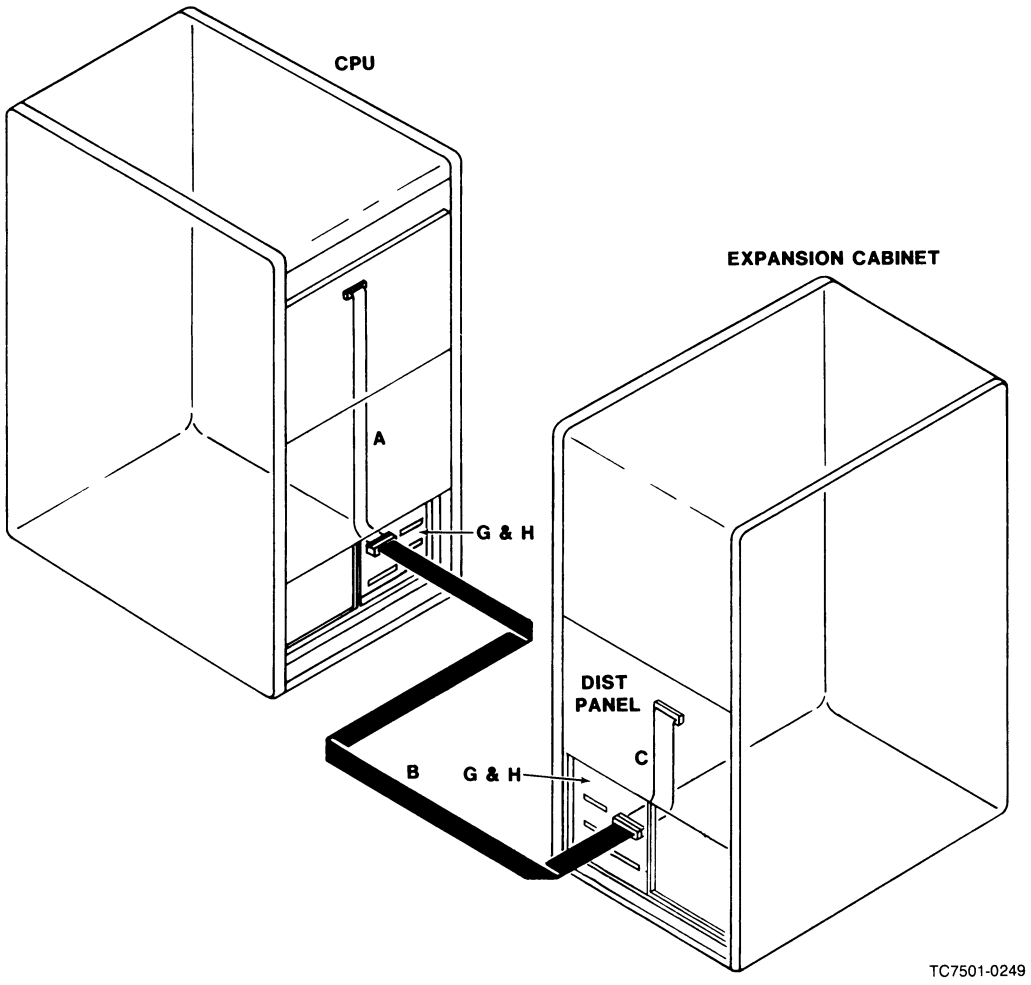

Figure 3-1. Typical System Hook-up

3.2.3 EMULATIONS IN VAX-11/750 AND VAX-11/780

When the TC7000 Tape Coupler is used in the VAX-11/750 CPU system, or in the VAX-11/780 CPU system, it emulates a DEC RH750 Massbus Adapter (MBA) or RH780 MBA, respectively, up to eight TM03 formatters, each with one attached TU77 tape transport (if Pertec subsystem) or up to four TM03 formatters, each with one attached TU77 tape transport (if STC subsystem).

3.2.4 SUPPORTED TAPE TRANSPORTS

The TC7000 Tape Coupler can support and is compatible with the physical tape transports listed in Appendix B.

3.3 CONFIGURATION DEFINED

In the computer industry, the term **configuration** generally means the physical and logical arrangement of system components, and the manner in which those components relate to each other. Therefore, the term configuration has many possible inferences:

- Size (capacity, format, speed, data density)
- Cabling (what is connected together)
- Logical arrangement (which functions are combined on which components)
- Location (bus slot, local/remote, bus address, interrupt vector address, unit address),

and so on.

Many of these factors can be established by the user by using switches, PROMs, jumpers, or special cabling arrangements. Thus, the system configuration and function of a system is defined and determined by the user. With the TC7000 Tape Coupler, many physical tape transports can be used, and to the software each appears to be a TM03 Formatter with a TU77 tape transport slave (see Appendices A and B).

3.4 CONFIGURATION AIDS

Configuration aids consist of connectors, switches, PROMs, indicators, and jumpers.

3.4.1 CONNECTORS

Connectors J1 and J2 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in Normal operations.

3.4.1.1 V-MASTER Cconnectors

The SBI interface signals enter the V-MASTER backplane via header connectors J7 through J12 on the right-side edge of the backplane and exit via header connectors J1 through J6 on the left-side edge of the backplane. Pin/signal assignments for the VMI and SBI interfaces are listed in Section 8.

The two sets of header connectors on the V-MASTER backplane, associated with slots three and four, are for interfacing the Cable Paddleboard PCBAs with the TC7000 Tape Couplers or SC7000 Disk Controllers (or with one of each).

Connectors J13 and J14 are both used to carry -5.2 Vdc to or from the V-MASTER. Connector J15 connects the AC/DC Low harness to the V-MASTER. B-plus and ground are provided by using the two sets of studs below the J13, J14, and J15 connectors.

3.4.2 SWITCHES

The V-MASTER/780 Bus Interface PCBA has one DIP switch; SW1, which is used to select the TR number for the NEXUS (see subsection 4.5.1.5.1).

The V-MASTER/780 Bus Translator PCBA has one DIP switch; SW1, which is used to enable/disable early transfer request (TR) and continuous Clock generation (see subsection 4.5.1.5.2).

The TC7000 Tape Coupler PCBA contains five DIP switches reference designated SW1, SW2, SW3, SW4, and SW5, which are used to configure the TC7000 Tape Coupler for various tape speeds, densities, certain firmware options, MBA number, and arbitration level.

3.4.3 PROMS

The V-MASTER/780 Bus Interface PCBA has two control PROMs, 591 and 592, mounted in IC sockets U76 and U78, respectively.

The TC7000 Tape Coupler has six IC sockets, reference designated U24 through U29, for mounting data PROMs. These PROMs provide the firmware used by the TC7000 Tape Coupler. The PROM in IC socket U14 is used to control buffer addressing.

3.4.4 INDICATORS

Two light emitting diode (LED) indicators are mounted near the front edge of the TC7000 Tape Coupler PCBA. They provide the following indications:

FAULT - Steady illumination indicates unsuccessful Self-Test execution.

Regular flashing indicates successful Self-Test but formatter/tape transport(s) are not connected to system, or if connected, are not powered up and on line.

Regular flashing (VAX-11/780 only) during bootstrap operation or during run of microdiagnostic test program indicates continuous Clock not being generated (SW1-3 on Bus Translator PCBA is ON).

Extinguished indicates successful Self-Test with at least one tape transport connected, powered up and on line.

ACTIVITY - When lit, indicates Write or read activity is occurring on a selected tape transport.

Extinguished indicates no Write or Read operation is occurring on any tape transport.

3.4.5 JUMPERS

The TC7000 Tape Coupler has no jumpers itself, but jumpers are included on the CPU backplane (see subsections 4.4.1 and 4.5.1) and also on certain PCBAs in the tape transports. Proper arrangement of these jumpers must be considered when preparing the system CPU and tape transports to operate with the TC7000 Tape Coupler. Appendix B lists jumper arrangements for various tape transports supported by the TC7000 Tape Coupler.

3.5 OPTIMIZING PERFORMANCE

To optimize system performance, the system should be checked for the following conditions:

a. DEC Field Change Order (FCO) number RH750-R0001 incorporated in RH750 (see subsection 4.4.2)

b. Proper noise suppression provided (see subsection 4.7).

c. CPU jumpers properly placed (see subsection 4.4.1 and 4.5.1).

d. Proper termination (see subsections 4.5.2.5 and 4.5.5).

e. SBI headers in proper position (see subsection 4.6.4).

4.1 OVERVIEW

This section describes the step-by-step procedure for installation of the TC7000 Tape Coupler in a VAX-11/750 or VAX/VMS-11/780 CPU system. To serve as an outline for the procedure, this section is divided into eight component-oriented subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	Tape Transport Preparation
4.4	VAX-11/750 System
4.5	VAX-11/780 System
4.6	Backplane Cabling
4.7	Cable Routing and RFI Suppression
4.8	Testing

All steps in these procedures apply to all installations and applications, except for the differences in VAX-11/750 and VAX-11/780 procedures. If there is already a DEC RH750 or RH780 MBA in the system, ignore RH750 or RH780 reconfiguration procedures. If there is no DEC RH750 or RH780 MBA in the system, all applicable steps must be performed.

Emulex recommends this section be read in its entirety before installation procedures are begun.

4.1.1 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the TC7000 Tape Coupler PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI).

Each TC7000 Tape Coupler PCBA is a standalone unit that complies with FCC regulations and is designed to be embedded in a VAX-11/750 CPU cabinet or in a V-MASTER/780 card cage assembly which in turn is embedded in a VAX-11/780 CPU cabinet. When properly installed, the TC7000 Tape Coupler system does not cause compliant computers to exceed RFI limits for Class A equipment.

There are two possible configurations in which the TC7000 Tape Coupler system can be installed:

a. In the same cabinet as the DEC CPU.

b. In an expansion cabinet that is separate from the CPU cabinet.

To limit radiated RFI, DEC completely encloses the computer system components, that could radiate or conduct RFI, with a grounded metal shield. When installing system components, do nothing that could reduce the effectiveness of the shield. That is, when installation of the TC7000 Tape Coupler system [TC7000 Tape Coupler PCBAs, Cable Paddleboard PCBAs, Personality Panels, Blank Panels (if any), Bulkhead Distribution Panels (if any), tape transports, and shielded cables] is complete, no gap in the shielding that would allow RFI radiation or conduction can be allowed.

Conducted RFI is generally prevented by installing a filter in the ac line between the computer system and the ac source. Most power distribution panels of current manufacture contain suitable filters.

The procedures required to maintain shield integrity and to limit radiated and conducted RFI are explained fully in subsection 4.7.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the system, visually inspect all assemblies for bent or broken connector pins, damaged components, or other visual evidence of physical damage or incomplete assembly such as missing hardware. The PROMs should be carefully examined to ensure each is firmly and completely seated in its proper socket. Verify that unit model or part number designation, revision level, and serial number agree with those on shipping invoice. This verification is important to confirm warranty. If evidence of physical damage, missing parts, or identity mismatch is found, notify an Emulex representative immediately.

4.3 TAPE TRANSPORT PREPARATION

Unpack and install the tape transports as instructed in the manufacturer's manual. Position and level them in their final places before beginning installation of the TC7000 Tape Coupler. This positioning allows input/output (I/O) cable routing and length requirements to be accurately determined. To simplify installation

and minimize I/O cable length, tape transports should be side-by-side.

Configure tape transport(s) for desired operating mode by using switches on operator control panel (OCP) of tape transport, or by issuing appropriate commands via software. For instance, PE operation on a dual-density NRZI/PE tape transport may be enabled by placing the high density (HI DEN) switch in the OCP of the tape transport in the ON position, or by setting the appropriate density bit code in register TMCR bits <10:08> of the TC7000 Tape Coupler via software instructions (after the TC7000 Tape Coupler is installed). Tape transport tape speed and density selection are matched on the TC7000 Tape Coupler when configuration is done.

4.3.1 TAPE TRANSPORT ADDRESSING

Up to eight tape transports may be daisy chained with the TC7000 Tape Coupler. Each tape transport must be assigned a unique unit address (select) number by selecting appropriate switch settings on the appropriate PCBA or the OCP of the tape transport. The unit address number on each tape transport must be different and must be within the range from zero to seven. Daisy chains with tape transports that have STC interfaces may only include up to four tape transports and have unit address numbers within the range from zero to three.

4.3.2 TAPE TRANSPORT MODIFICATIONS

In some applications, tape transports must undergo minor modifications before they can be used in the system (see Appendix B).

4.4 VAX-11/750 SYSTEM

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TO AVOID POSSIBLE PERSONAL INJURY OR CIRCUIT DAMAGE, **ALWAYS** VERIFY CPU POWER IS OFF BEFORE REMOVAL OR REPLACEMENT OF ANY SYSTEM PCBA.

Power down the system by placing the main AC circuit breaker at the rear of the CPU cabinet in the OFF position. The AC indicator lamp should remain lit. Open the front door of the CPU cabinet and remove the card-rack cover. Open the rear door of the CPU cabinet and remove the backplane cover. The interior of the CPU cabinet is then accessible to the user.

4.4.1 BUS GRANT JUMPER REMOVAL

To remove applicable Bus Grant jumpers from the CPU backplane, see Figure 3-1 and use the following procedure:

a. Locate Bus Grant jumpers for option slots seven, eight and nine on CPU backplane.

b. Remove Bus Grant jumpers from slot in which TC7000 Tape Coupler is to be installed.

c. If a controller is already present in one of the option slots, the Bus Grant jumpers for that slot should already have been removed; if not removed, remove them now.

d. Save removed Bus Grant jumpers.

4.4.2 RH750 MBA RECONFIGURATION

If a DEC RH750 Massbus Adapter (MBA) is present in the system and located in option slot nine, Emulex recommends moving the RH750 MBA to slot eight or seven. CMI Bus addressing is not related to the slot in which the TC7000 Tape Coupler is placed, so the RH750 MBA can remain the bootstrap device if desired.

If the RH750 MBA is not located in option slot nine, it is not necessary to move it; however, it may be necessary to select a different bus arbitration level if the Field Change Order (FCO) described in the following paragraphs has not been applied.

Before removing the RH750 MBA from the card rack, determine whether FCO #RH750-R0001 has or has not been installed. If this FCO has been installed, the new revision number for the RH750 MBA should be A1 and should be indicated by Brady markers on the module handle (outside edge of the PCBA). Also check the Engineering Change Order (ECO) and FCO section of the Site Management Guide for your VAX-11/750 CPU to determine if the FCO implementation record has been entered. This FCO cures the tendency of the RH750 MBA to seize and hold the CMI Bus by asserting its arbitration signal for extended periods. If not cured, this problem causes other Massbus devices that have lower arbitration levels to generate Data Late errors. Emulex recommends this FCO be applied before a second Massbus device (such as the TC7000 Tape Coupler) is installed in the system.

If it is not possible for this FCO to be applied before the installation of the Emulex TC7000 Tape Coupler, the RH750 MBA must be reconfigured to a CMI Bus arbitration level that is lower than that of the TC7000 Tape Coupler so as to prevent Data Late error conditions (see subsection 4.4.4).

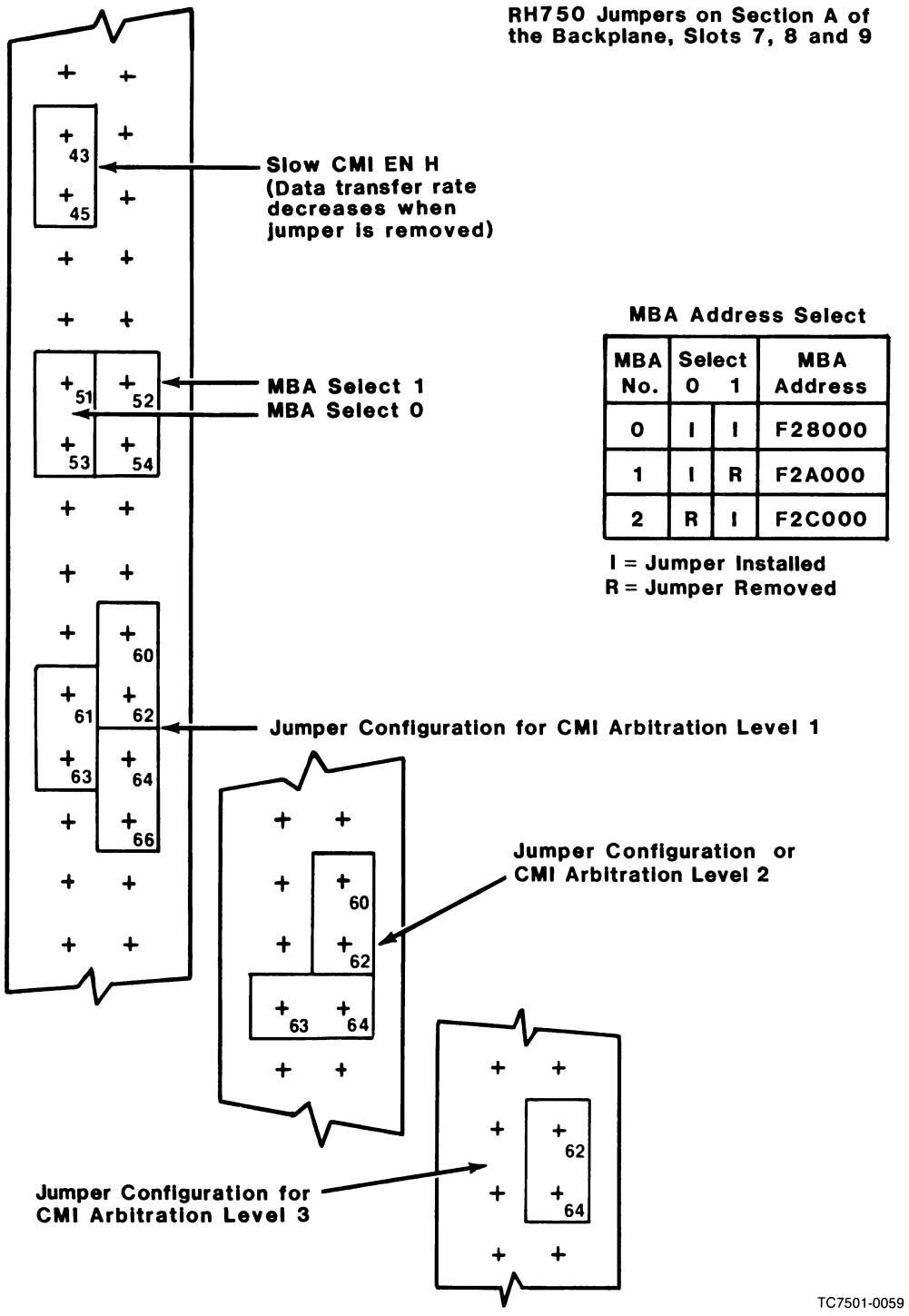


Figure 4-1. Jumpers in CPU Backplane for RH750 MBA

4.4.3 RH750 MBA REMOVAL

Remove the RH750 MBA from option slot nine. If FCO #RH750-R0001 has not yet been applied to the RH750 MBA module, do so now. Insert the RH750 MBA in either option slot eight or seven.

4.4.4 RH750 BACKPLANE RECONFIGURATION

To reconfigure the CPU backplane for the requirements of FCO #RH750-R0001, see Figure 4-1 and use the following procedure:

a. Record jumper arrangement, then remove from option slot nine, on CPU backplane, the following jumpers:

   SLOW CMI EN H
   MBA SELECT 0
   MBA SELECT 1
   CMI ARBITRATION (ARB) LEVEL 1
   CMI ARB LEVEL 2
   CMI ARB LEVEL 3

b. Place SLOW CMI EN H jumper in same relative location on CPU backplane of new slot chosen for RH750 MBA.

c. If RH750 MBA is to remain as bootstrap device (address F28000), place both MBA SELECT jumpers in same relative location on new slot. If Emulex TC7000 Tape Coupler is to become new bootstrap device, select either F2A000 or F2C000 as address for RH750 MBA.

d. Determine arbitration level assigned to original RH750 MBA installation (see Figure 4-1).

e. If FCO #RH750-R0001 has been installed and RH750 MBA is to remain bootstrap device, place CMI ARB jumper(s) in same relative location on new slot.

f. If FCO has not been applied and arbitration level three has been assigned, select a lower CMI ARB level (two or one). This selection must be done whether the RH750 MBA is or is not being moved. Bus Grant jumpers removed in step a may be used to select lower CMI ARB level.

g. Remove three Massbus plugs from sections B and C of backplane and set them on top of card rack.

h. When I/O cables for TC7000 Tape Coupler have been installed on Cable Paddleboard PCBA, plug these three Massbus plugs into same relative location in new CPU backplane slot for RH750 MBA.

4.4.5 TC7000 TAPE COUPLER CONFIGURATION IN VAX-11/750 CPU

Selection of the Base Address and Arbitration Level is done by setting switches in DIP switch packs. Component locations on the TC7000 Tape Coupler are shown in Figure 4-2.

4.4.5.1 DIP Switch Types

DIP switches used in this product may be any one of three types shown in Figure 4-3.

Switch-setting tables in this manual use the numeral one (1) or the letter (C) to indicate the ON (CLOSED) position and the numeral zero (0) or the letter (O) to indicate the OFF (OPEN) position.

4.4.5.2 MBA Number Selection

The MBA number represents the Base Address on the CMI Bus and the Interrupt Vector Address for the TC7000 Tape Coupler. DIP switches SW5-7 and SW5-8 are used for this selection. If the tape transport which is to be used to bootstrap the system on power up is connected to the TC7000 Tape Coupler, then the TC7000 Tape Coupler must use the Base Address F28000. This selection has no effect on the arbitration level which is set as described in subsection 4.4.5.3. Switch positions for MBA number selection are listed in the following table:

Switch SW5-7	Switch SW5-8	Base Address	Interrupt Vector Address	MBA Device Number
O	O	F28000	150	RH0
O	C	F2A000	154	RH1
C	O	F2C000	158	RH2
O = Open		C = Closed		

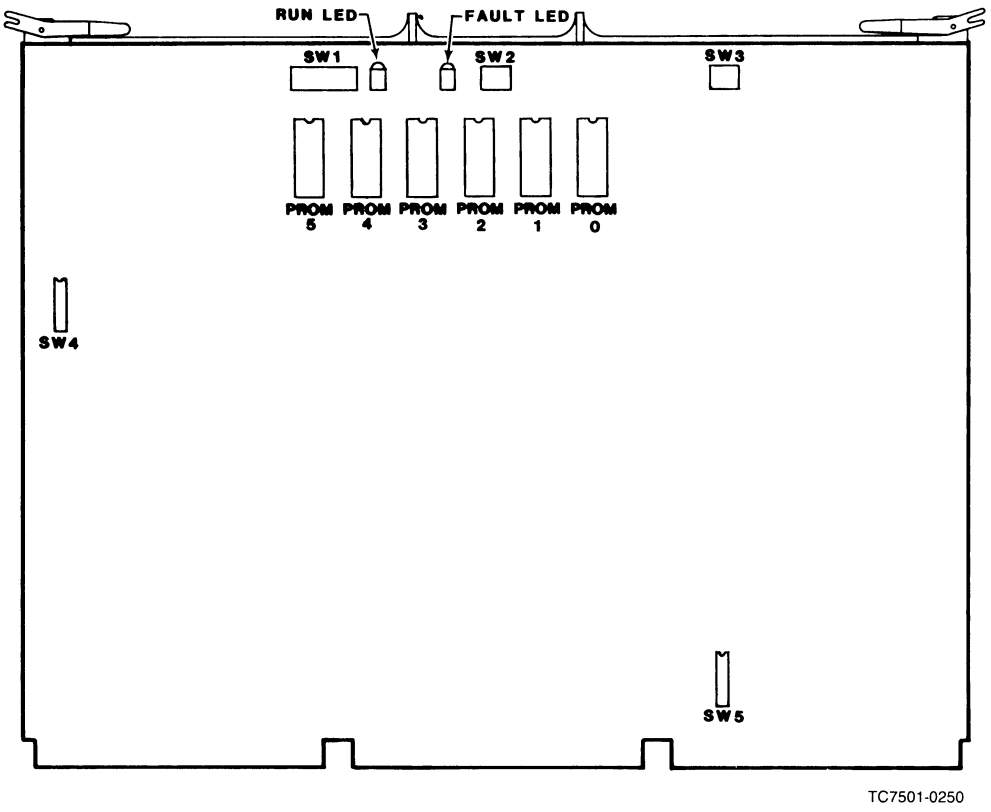
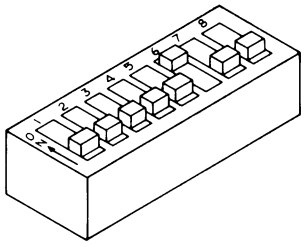
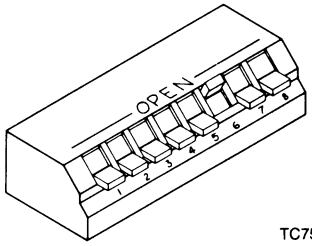


Figure 4-2. TC7000 Tape Coupler PCBA, Component Locations



Slide Switch:
To place a slide switch in the ON position, simply slide the switch in the direction marked On or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direction marked OFF or OPEN.



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Piano Switch:
To place a piano switch in the ON position, press the switch. To place a piano switch in the OFF position, raise the switch.

Figure 4-3. DIP Switch Types

4.4.5.3 Arbitration Selection

The arbitration level (CMI Bus Priority Level) is selected by switches in DIP switch pack SW5, as listed in the following table:

Level	DIP Switch SW5- 2	3	4	5	6	Rank
3	C	O	O	O	O	Highest MBA Level
2	O	C	O	C	O	
1	O	O	C	C	C	Lowest MBA Level
O = Open				C = Closed		

Each Massbus device must be assigned a unique arbitration level. If the system includes a DEC RH750 MBA, the arbitration level of that RH750 MBA must be determined by inspecting the position of the Bus Grant jumpers on the CPU backplane. If those jumpers have not yet been properly configured (see subsection 4.4), they should be so configured now. If the DEC FCO has been applied (see subsection 4.5), select any one of the arbitration levels that is not being used. If the FCO has not been applied, select a higher arbitration level than that given to the RH750 MBA.

4.4.5.4 Tape Transport Configuration Selection

Tape transport configuration selection for the TC7000 Tape Couplers installed in the VAX-11/750 CPU systems is the same as for those installed in the V-MASTER/VAX-11/780 CPU system (see Appendix B).

4.4.5 5 Option Switches

This configuration selection is the same as described for TC7000 Tape Couplers in V-MASTER/VAX-11/780 CPU systems (see Appendices A and B).

4.4.6 CABLE PADDLEBOARD INSTALLATION IN VAX-11/750 CPU

One Cable Paddleboard PCBA is required for each TC7000 Tape Coupler. In the VAX-11/750 CPU system, this PCBA is installed on the backplane of the option slot that is to contain the TC7000 Tape Coupler.

NOTE

Cable Paddleboard PCBA installation procedures in this manual assume the TC7000 Tape Coupler PCBA is installed in slot 9 of the VAX-11/750 CPU with the Cable Paddleboard PCBA installed on the corresponding backplane. These procedures also assume the view is from the rear and toward the backplane.

To install the Cable Paddleboard PCBA on the VAX-11/750 CPU backplane, see Figures 4-4 and 4-5 and use the following procedure:

a. Verify CPU power is OFF.

b. Remove Phillips-head screw, located to right side of backplane slot 10 between sections B and C.

c. Install support bracket (Emulex Kit P/N SC7513101) on Cable Paddleboard PCBA.

d. Plug tape transport interface cables into appropriate connectors on Cable Paddleboard PCBA. These six connectors are on left side of PCBA. Connectors J1 and J2 provide cable connections to interface Pertec tape transports with the TC7000 Tape Coupler. Connectors J3 through J6 provide cable connections to interface STC tape transports with the TC7000 Tape Coupler.

e. Carefully position three connectors on Cable Paddleboard PCBA over backplane connector pins (sections B and C) of slot 10 so that white guide between top and middle connectors is between bottom two pins of section B and

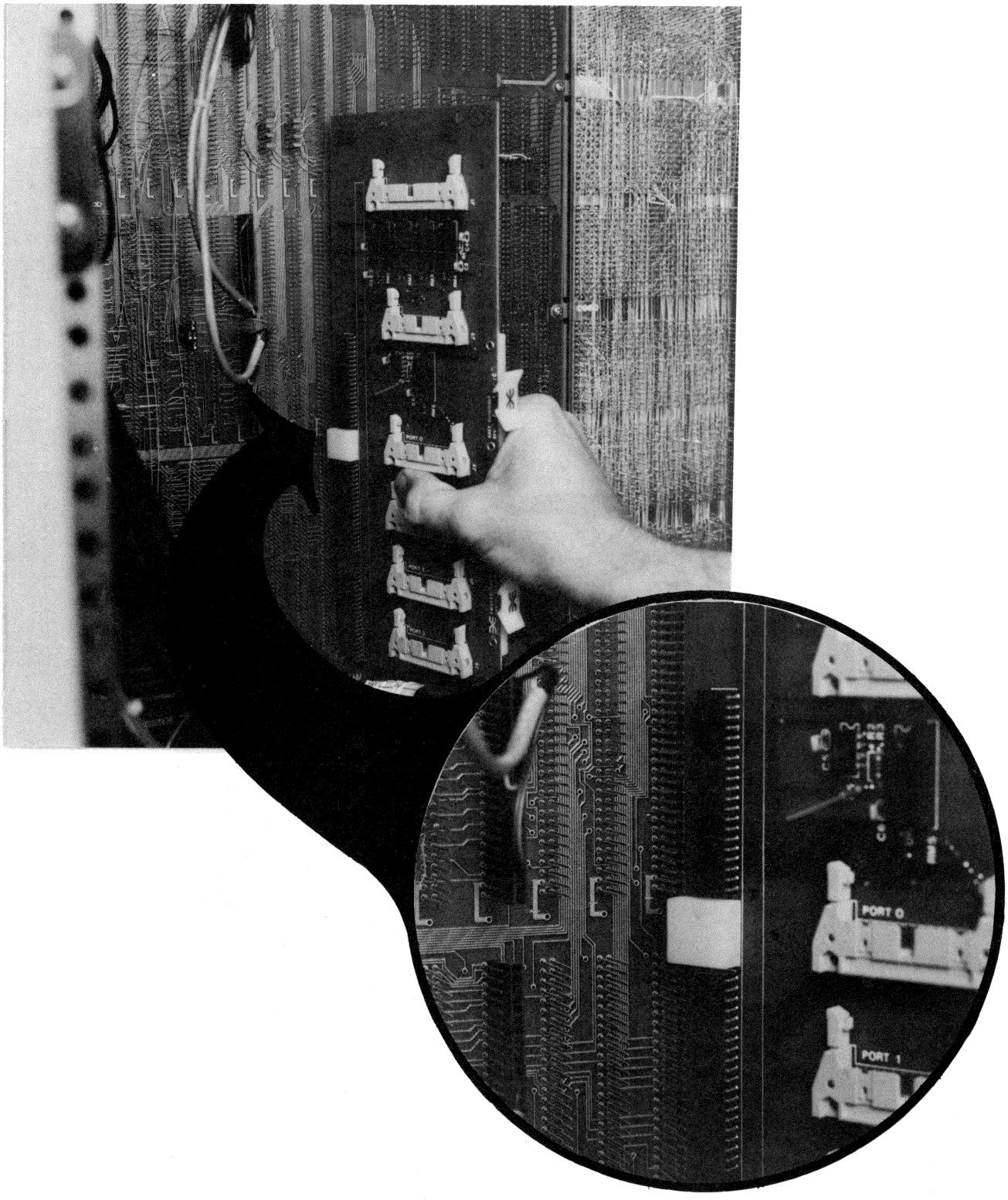

Figure 4-4. Cable Paddleboard PCBA Installation
(stiffener removed for clarity)

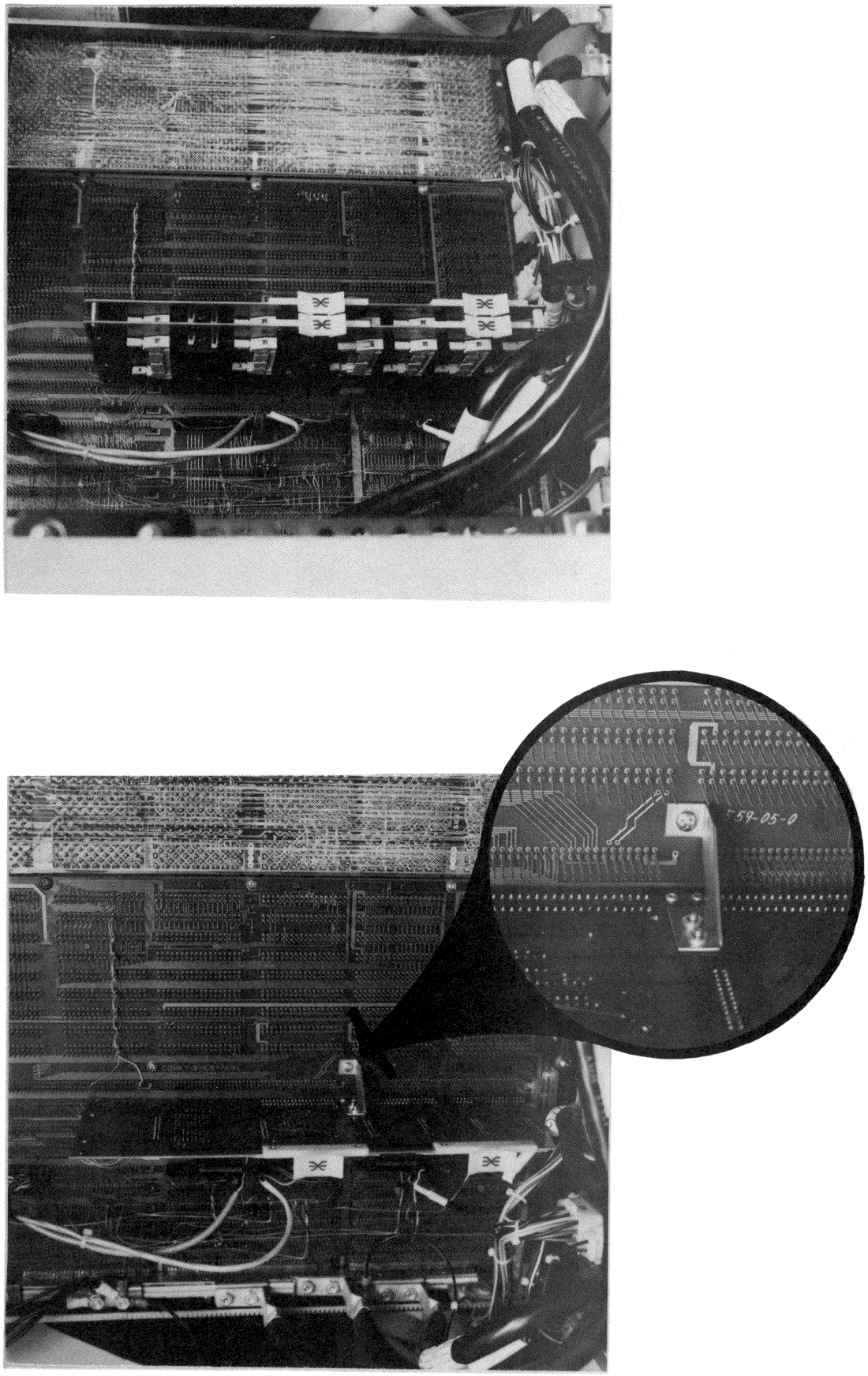

Figure 4-5. Single and Dual Cable Paddleboard PCBA Installation Details

top two pins of section C, and at same time rest PCBA against pins at right side of backplane connector. When position of PCBA looks and feels as if backplane pins can properly engage connectors on PCBA, gently push PCBA forward until it bottoms on backplane header. When PCBA is properly seated, black alignment guides should be sandwiched between connectors on PCBA and backplane header.

f. Insert screw, removed in step a, through support bracket and tighten in place.

g. Attach subsequent Cable Paddleboard PCBAs to the first one using a standoff (Emulex part number SC7513102) which mates to the standoff on the first Paddleboard.

4.4.7 TC7000 TAPE COUPLER INSTALLATION IN VAX-11/750 CPU

The TC7000 Tape coupler may be installed in slot seven, eight, or nine in the CPU backplane. Any of these three slots not already occupied may be used, but slot nine is best for ease of Cable Paddleboard PCBA installation. To install the TC7000 Tape Coupler in the VAX-11/750 CPU cabinet, use the following procedure:

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TO AVOID POSSIBLE PERSONAL INJURY OR CIRCUIT DAMAGE, **ALWAYS** VERIFY CPU POWER IS OFF BEFORE REMOVAL OR REPLACEMENT OF ANY SYSTEM PCBA.

a. Position PCBA so that component side faces in same direction as component side of other PCBAs already installed in CPU cabinet.

b. Verify PCBA is properly positioned in throat of each connector before attempting to seat PCBA in connectors.

c. Gently but firmly push extractor handles on PCBA with even pressure until PCBA is fully seated on connector header.

NOTE

To remove any PCBA in system, raise extractor handles until handles are erect, then slide PCBA from mounting slot.

4.5 VAX-11/780 SYSTEM

Before installation of an additional NEXUS such as V-MASTER, DEC MBA, or DEC UBA, the TR level and address range of all previously

installed NEXUSes must be determined to prevent new devices from having the same TR level or addresses which are presently in use.

DEC TR levels are normally associated with the various NEXUS address ranges, as listed in Table 4-1. For DEC MBAs, the TR level and the address range are selected separately.

Table 4-1. Setting Numbers for Base Address and TR Level

Base Address	TR Level	Setting Number	Base Address	TR Level	Setting Number
20008000	TR4	3	20010000	TR8	7
2000A000	TR5	4	20012000	TR9	8
2000C000	TR6	5	20014000	TR10	9
2000E000	TR7	6	20016000	TR11	10

To determine the Base Address for a particular MBA, a combination of pin/plugs at the top of the DEC MBA chassis backplane is used. The pin/plugs are weighted, starting with the leftmost pair of pins and counting four pairs to the right: eight, four, two, and one. The sum of the pin/plugs equals the setting number for the desired Base Address, as listed in Table 4-1; e.g., if the desired Base Address is 20010000, pin/plugs four, two and one would be installed.

Pins to the right of these four pairs are used to select the Bus Request (BR) level. It is not necessary to determine the BR level of the RH780 MBA or to select a different BR level for the V-MASTER/780.

A jumper wire on the CPU backplane of the second PCBA slot determines the TR level. The different jumper positions are listed in the following table:

F2F1 to F2C1 = TR1		F2F1 to F2J2 = TR7	
F2F1 to F2D1 = TR2		F2F1 to F2M1 = TR8	
F2F1 to F2E1 = TR3		F2F1 to F2N1 = TR9	
F2F1 to F2F2 = TR4		F2F1 to F2P1 = TR10	
F2F1 to F2H2 = TR5		F2F1 to F2P2 = TR11	
F2F1 to F2J1 = TR6		F2F1 to F2S2 - TR12	

The RH780 MBA backplane is shown in Figure 4-6. In this figure, letters are included to help identify pin locations, although the letters are not actually on the RH780 MBA backplane. The numbers on the backplane do not appear in the same location as shown in Figure 4-6; they are located near the center of the PCBA, not directly above block "F". The letters are added and the numbers shown mislocated to make pin identification easier.

Jumper pin locations are defined by a series of numbers and letters which designate block, column and row. The first letter designates the block. The blocks of pins are lettered in sequence, beginning with block "A" at the top and proceeding to block "F" at the bottom (six blocks). The next character in the pin identification code is a number that designates a column which is four pins wide; therefore, the first four pins at the left are in column one. The next character is a letter that designates a row of pins. Each row is labeled in Figure 4-6, and each row of pins is offset from the

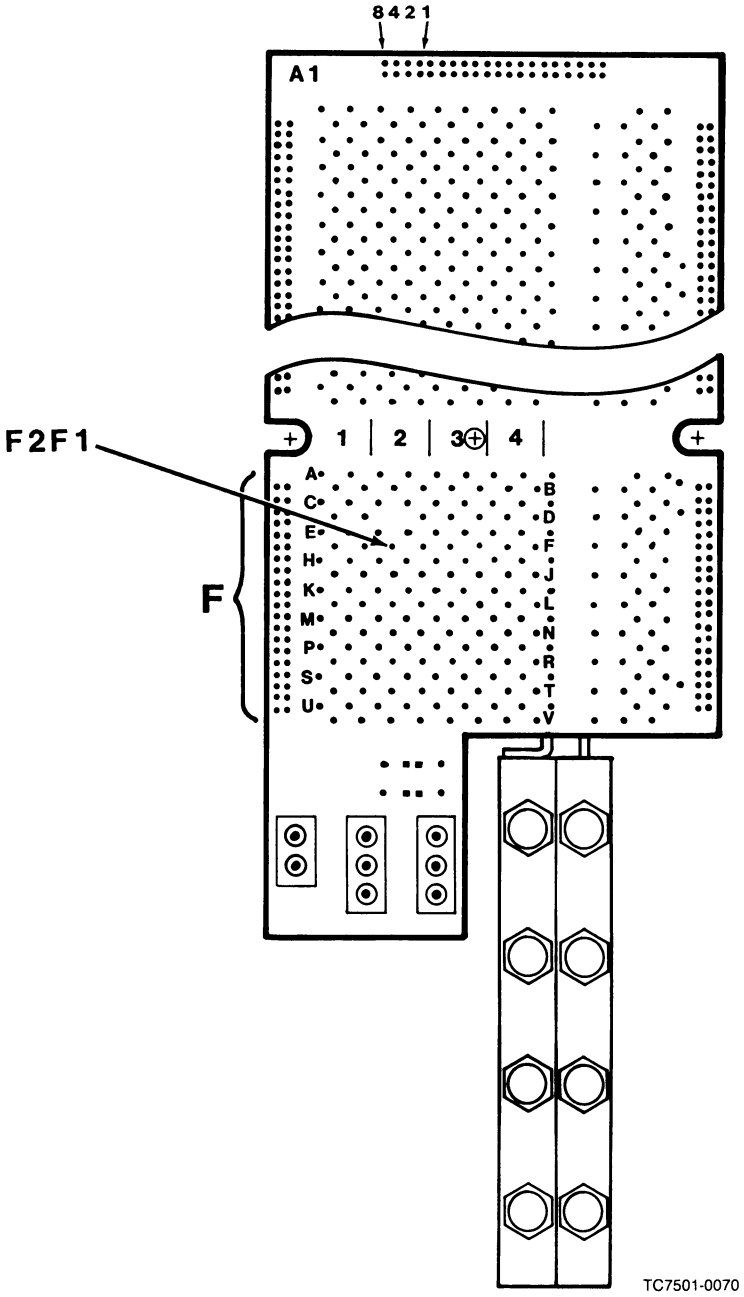

Figure 4-6. RH780 MBA Backplane

row above and below. The last character is a number that designates which of two pins in the same row is designated by the same column number. A number "1" designates the left-side pin of that column in a particular row, and a number "2" designates the right-side pin. In Figure 4-6, pin F2F1 is indicated by an arrow.

Normally, changing the TR level of an installed DEC RH780 MBA is not necessary; i.e., having the V-MASTER/780 at a lower TR level (TR10 or TR11) is desirable because the TC7000 Tape Coupler has a 512-byte buffer.

4.5.1 V-MASTER/780 PREPARATION

The V-MASTER/780 assembly consists of a wire chassis and an Emulex VMI Bus backplane that can accept four hex-sized PCBAs. Two of the PCBA slots are for the hardware needed to mate the DEC SBI with the Emulex TC7000 Tape Couplers (Emulex P/N TU7510401). The Bus Interface PCBA (Emulex P/N SU7810401) and the Bus Translator PCBA (Emulex P/N SU7810409) are part of the completed V-MASTER/780 assembly. Procedures for reconfiguring these two PCBAs for particular applications are described in the next four subsections. The remaining two hex-sized PCBA slots in the V-MASTER/780 chassis are for installation of one or two Emulex controllers in any combination (TC7000s, SC7000s, SC788s, or SC780s).

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TO AVOID POSSIBLE PERSONAL INJURY OR CIRCUIT DAMAGE, **ALWAYS** VERIFY CPU POWER IS OFF BEFORE REMOVAL OR REPLACEMENT OF ANY SYSTEM PCBA.

4.5.1.1 Bus Interface PCBA Removal

To gain access to DIP switch SW1 on the Bus Interface PCBA, that PCBA must be temporarily removed. To remove the PCBA, raise the extractor handles, then gently lift the PCBA from the slot. Switch SW1 is used to configure SBI Arbitration level and SBI Interrupt Request level.

4.5.1.2 SBI Arbitration (TR Number) Level

Each NEXUS on the SBI is assigned a Transfer Request (TR) number which represents its arbitration level. The TR number correlates to the Base Address of the TC7000 Tape Coupler. The MBA controller's are normally assigned addresses in the range from TR8 to TR11, although the TC7000 Tape Coupler can handle numbers from TR4 through TR11. (The DEC MBA device is usually assigned to TR8.) The TC7000 Tape Coupler with the even-numbered address is normally installed in slot three, and the other TC7000 Tape Coupler (odd number) is assigned to slot four. This even-odd arrangement is applicable only to dual-tape coupler installations; a single TC7000 Tape Coupler can be in either slot three or four and have either an

even or odd TR level selected. The TR level number is assigned by DIP switches SW1-1 through SW1-4. Switch settings are listed in Table 4-2, and component locations on the Bus Interface PCBA are shown in Figure 4-7.

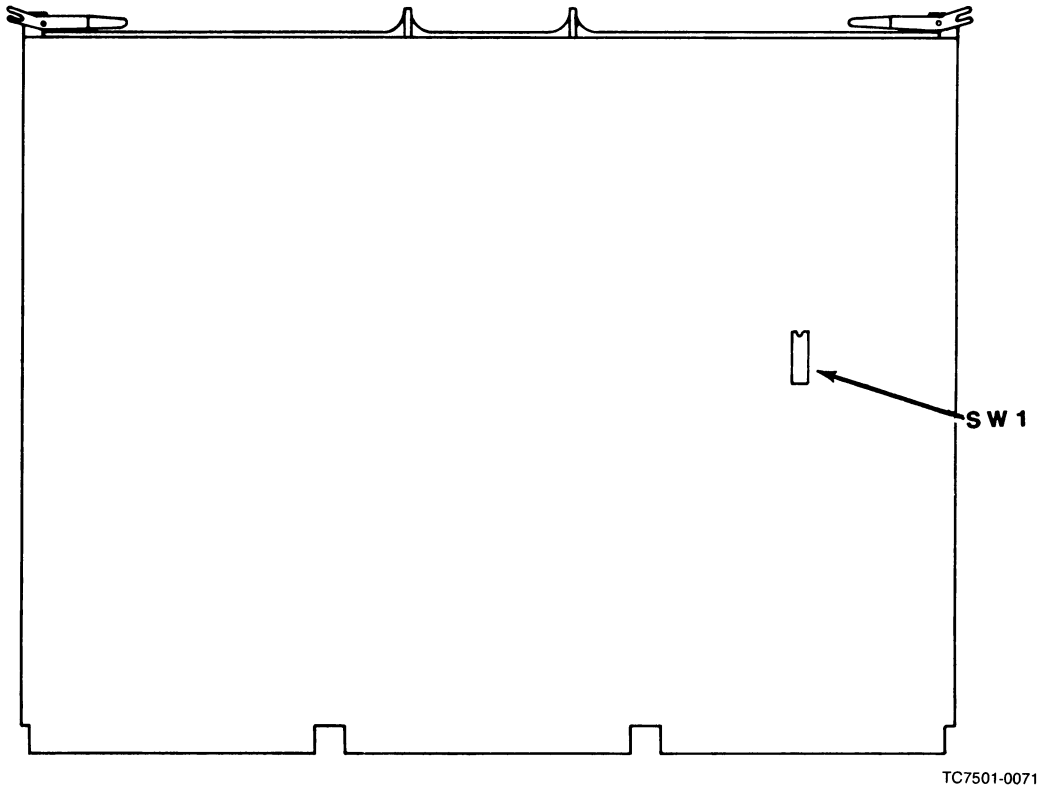


Figure 4-7. Bus Interface PCBA, Component Locations

Table 4-2. DIP Switch Settings for TR Level

TR Level	SW1- 4	3	2	1
4	O	C	O	O
5	O	C	O	C
6	O	C	C	O
7	O	C	C	C
8	C	O	O	O
9	C	O	O	C
10	C	O	C	O
11	C	O	C	C

O = Open C = Closed

4.5.1.3 SBI Interrupt Request Level

The one or two TC7000 Tape Couplers are assigned Interrupt Request levels by DIP switches SW1-5 and SW1-6 on the Bus Interface PCBA. Normally, level five should be used. Switch settings are listed in Table 4-3.

Table 4-3. DIP Switch Settings for Interrupt Request Level

Level	SW1-6	SW1-5
4	O	O
5	O	C
6	C	O
7	C	C

4.5.1.4 Bus Interface PCBA Installation

The Bus Interface PCBA is installed in slot one of the V-MASTER/780 chassis; i.e., right-side slot as viewed from front. The Bus Translator PCBA is installed in slot two. Component side of PCBAs should face same direction as on other PCBAs installed in CPU chassis. To reinstall the Bus Interface PCBA after setting DIP switches, carefully insert PCBA in throat of connector slots. Verify PCBA is properly positioned in throat, then seat PCBA by firmly pressing down on extractor handles.

4.5.1.5 Bus Translator PCBA

The Bus Translator PCBA includes DIP switch SW1 at the front edge, as shown in Figure 4-8. SW1 is accessible without removing the PCBA from the V-MASTER, and it enables selection of two features: Early Transfer Request and Continuous Clock Generation.

4.5.1.5.1 Early Transfer Request. When DIP switches SW1-1 and SW1-2 are placed in the ON (CLOSED) position, early TR arbitration for the TC7000 Tape Couplers in V-MASTER slots three and four, respectively, is enabled. This feature asserts the TR level of the V-MASTER 800 nanoseconds before an SBI command is issued. Early TR assertion prevents any nexus, which has a lower priority than the V-MASTER, from using the SBI bus. If no other nexus with a higher arbitration level requests the SBI bus after the TR level of the V-MASTER is asserted, the V-MASTER uses the SBI bus for its Data Transfer operation. Since the CPU is always set for the lowest arbitration level (TR15), a small amount of processing time is lost

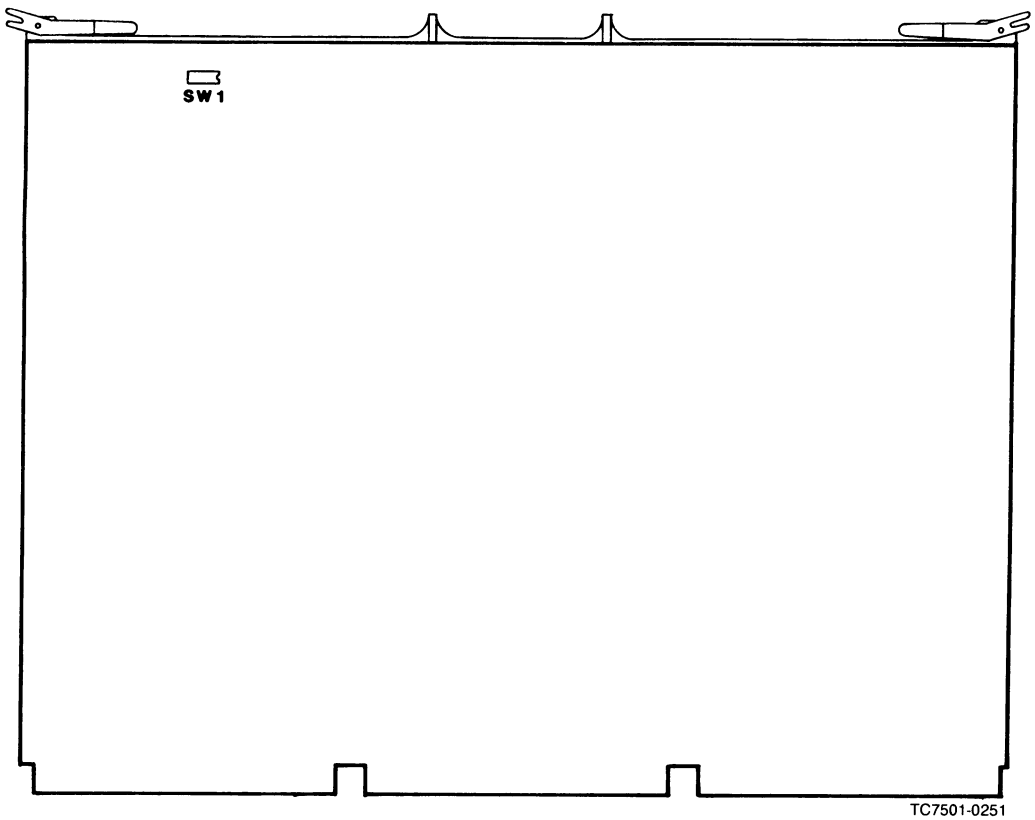


Figure 4-8. Bus Translator PCBA, Component Locations

when this feature is enabled. The amount of time lost depends on the type of Memory Controller module installed in the system and on the intensity of CPU or I/O processing. The user should run a benchmark test to determine if this feature is or is not desirable for the system. Early TR arbitration may be useful to users of tape transports that have high Data Transfer rates.

4.5.1.5.2 Continuous Clock Generation. When DIP switch SW1-3 is placed in the OFF (OPEN) position, continuous Clock generation is enabled for both controllers in the V-MASTER, and the FAULT LED on each controller PCBA remains unlit during a system bootstrap operation, or during the running of micro-diagnostic test programs. When switch SW1-3 is ON (CLOSED), the controllers in the V-MASTER lack continuous Clock generation and the FAULT LED on each controller PCBA blinks during a system bootstrap operation or during the running of micro-diagnostic test programs.

4.5.2 TC7000 TAPE COUPLER CONFIGURATION IN VAX-11/780 CPU

One or two TC7000 Tape Coupler PCBAs may be plugged into the SBI Bus created by the Bus Interface and Bus Translator PCBAs in the V-MASTER/780 assembly. The TC7000 Tape Couplers need to be configured for the particular intended application. This subsection describes those configuration procedures. Because not all DIP switches on the TC7000 Tape Coupler are readily accessible after the TC7000 Tape Coupler PCBA is installed in the V-MASTER/780 card cage assembly, configuration should be done before such installation.

4.5.2.1 TC7000 Tape Coupler Base Address

The Base Address of the TC7000 Tape Coupler is selected with respect to the V-MASTER/780 slot in which the TC7000 Tape Coupler PCBA is installed. DIP switch pack SW5 is used, as listed in Table 4-4. For single PCBA installations, slot number three should be used so that installation of the associated Cable Paddleboard PCBA can be more easily done.

Table 4-4. DIP Switch Settings for Base Address and VMI Arbitration Level

Coupler Position	SW5- 1	2	3	4	5	6	7	8
Slot 3 (R)	C	O	C	O	O	O	O	O
Slot 4 (L)	C	O	O	C	C	O	O	C
O = Open			C = Closed					

4.5.2.2 Arbitration Level

The TC7000 Tape Coupler must be assigned VMI Arbitration Level two or one, depending on the slot in which it is to be installed. Slot three is right-side slot and slot four is left-side slot when viewed from the front of the V-MASTER/780 card cage assembly. Systems with a single TC7000 Tape Coupler can use either slot, but slot three should be used (see subsection 4.5.1.2). DIP switch settings for the VMI Arbitration Level are included in Table 4-4.

NOTE

VMI Arbitration Level setting is not related to SBI Arbitration Level described in subsection 4.5.1.2.

4.5.2.3 Tape Transport Configuration Selection

Tape transport configuration selection for the TC7000 Tape Couplers installed in V-MASTER/VAX-11/780 CPU systems is the same as for TC7000 Tape Couplers installed in the VAX-11/750 CPU system (see Appendix B).

4.5.2.4 Option Switches

This configuration selection is the same as described for TC7000 Tape Couplers in VAX-11/750 CPU systems (see Appendices A and B).

4.5.2.5 Emulex Bus Terminator

If the V-MASTER/780 assembly is to be installed in the termination slot of the VAX-11/780 CPU chassis, the Emulex Bus Terminator PCBA (Emulex P/N SU7810406) must be installed on the V-MASTER/780 backplane. The Emulex Bus Terminator is electrically identical to the standard DEC Bus Terminator. To install the Bus Terminator PCBA, see Figure 4-9 and use the following procedure:

a. Remove two Phillips-head screws, located to right of bus-out pins and between sections of slot one, as viewed from rear of V-MASTER/780 card cage assembly.

b. Install Bus Terminator PCBA on bus-out pins at left edge of V-MASTER/780 backplane connectors J1 through J6. Verify connectors of Bus Terminator PCBA are fully seated on bus-out pins of backplane.

c. When Bus Terminator PCBA is properly seated on bus-out pins of backplane, replace screws, removed in step a, by inserting them through holes in support bracket for Bus Terminator PCBA. Tighten screws.

d. Connect power supply cables to appropriate jacks on Emulex Bus Terminator PCBA. Jacks have same reference designators as jacks on DEC Bus Terminator PCBA and power supply cables are connected in same way on Emulex Bus Terminator PCBA as on DEC Bus Terminator PCBA (see subsection 4.6).

4.5.3 CABLE PADDLEBOARD INSTALLATION IN V-MASTER

One Cable Paddleboard PCBA is required for each TC7000 Tape Coupler. In the VAX-11/780 CPU system, this PCBA is installed on the backplane of the appropriate slot in the V-MASTER/780 card cage assembly.

NOTE

Cable Paddleboard PCBA installation procedures in this manual assume the TC7000 Tape Coupler PCBA is installed in slot 3 of the V-MASTER/780 card cage assembly, with the Cable Paddleboard PCBA installed on the corresponding backplane. These procedures also assume the view is from the rear and toward the backplane.

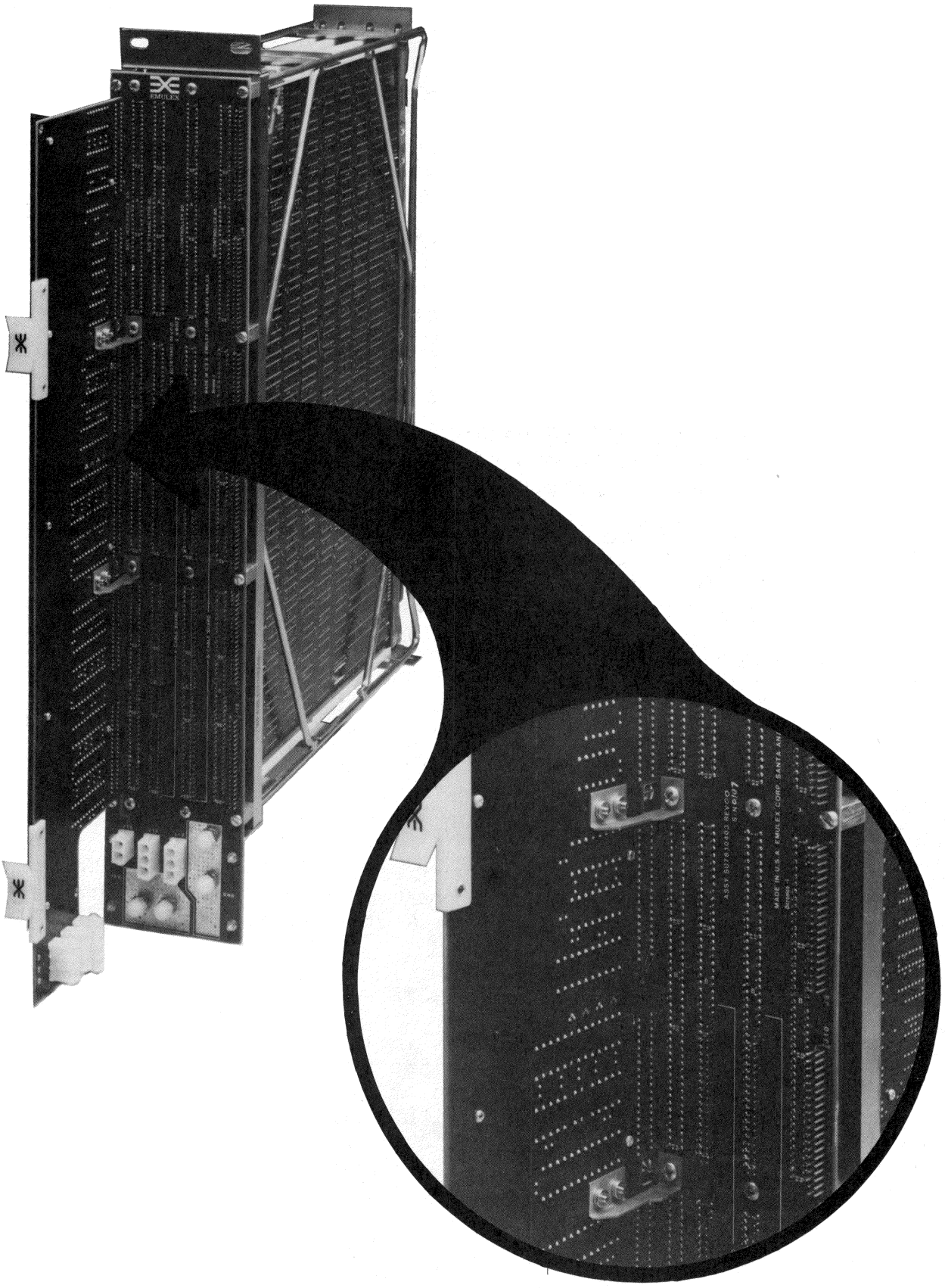


Figure 4-9. Emulex Bus Terminator PCBA Installation

To install the Cable Paddleboard PCBA on the V-MASTER/780 backplane, see Figures 4-10 and 4-11 and use the following procedure:

a. Remove Phillips-head screw, located to right side of backplane slot three between sections B and C.

b. Install support bracket (Emulex Kit P/N SC7513101) on Cable Paddleboard PCBA.

c. Plug tape transport interface cables into appropriate connectors on Cable Paddleboard PCBA. These six connectors are on left side of PCBA. Connectors J1 and J2 provide cable connections to interface Pertec tape transports with the TC7000 Tape Coupler. Connectors J3 through J6 provide cable connections to interface STC tape transports with the TC7000 Tape Coupler.

d. Do not remove black alignment guides at top of backplane headers.

e. Carefully position three connectors on Cable Paddleboard PCBA over backplane connector pins (sections B and C) of slot three so that white guide between top and middle connectors is between bottom two pins of section B and top two pins of section C; and at same time rest PCBA against pins at right side of backplane connector. When position of PCBA looks and feels as if backplane pins can properly engage connectors on PCBA, gently push PCBA forward until it bottoms on backplane header. When PCBA is properly seated, black alignment guides should be sandwiched between connectors on PCBA and backplane header.

f. Insert screw, removed in step a, through support bracket and tighten in place.

g. Attach subsequent Cable Paddleboard PCBAs to the first one using a standoff (Emulex part number SC7513102) which mates to the standoff on the first Paddleboard.

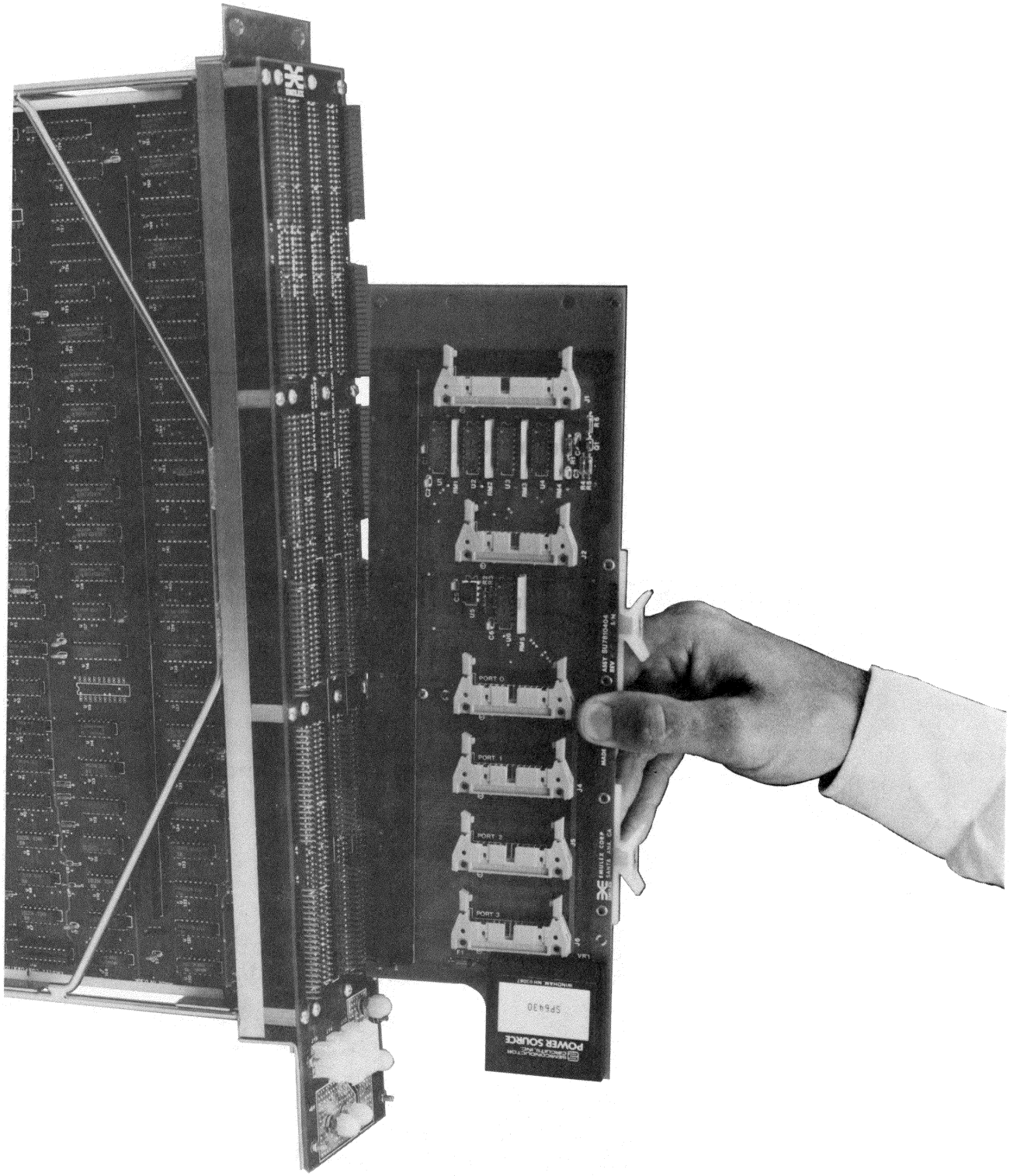


Figure 4-10. Cable Paddleboard PCBA Installation in V-MASTER/780 Card Cage

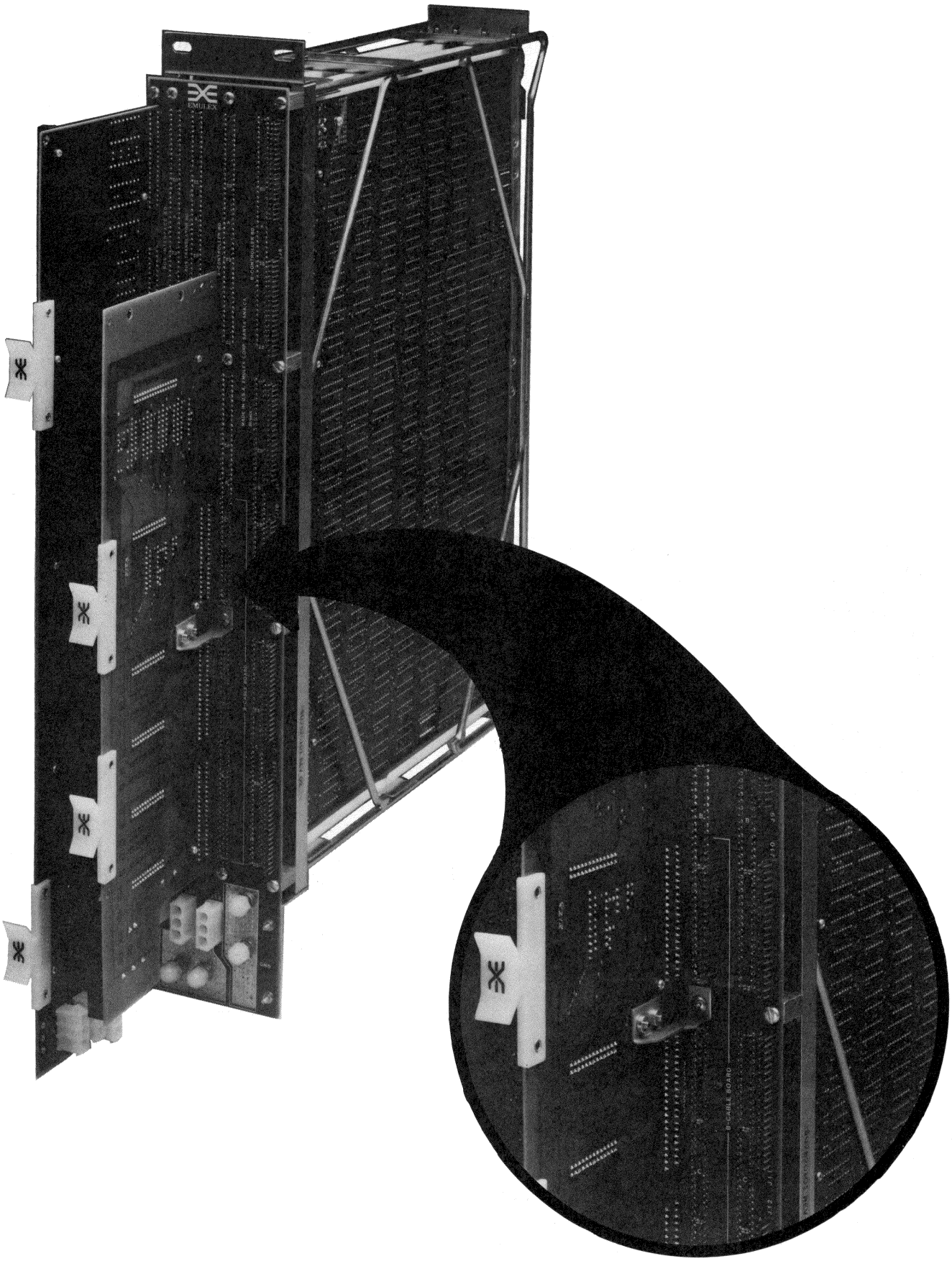


Figure 4-11. Cable Paddleboard PCBA Installation Detail

4.5.4 TC7000 TAPE COUPLER INSTALLATION IN V-MASTER/780 CARD CAGE

The TC7000 Tape Coupler may be installed in slot three or four of the V-MASTER/780 card cage assembly. To make installation of the Cable Paddleboard easy, slot three should be used. PCBA installation is the same as steps a, b, and c of subsection 4.4.7.

4.5.5 V-MASTER/780 INSTALLATION

The V-MASTER/780 card cage assembly may be installed in one of two locations in the VAX-11/780 CPU cabinet, or it may be installed in a DEC Expansion Box cabinet. In all installations, the V-MASTER/780 card cage assembly must contain all PCBAs, including interface cables for tape transports, before it is installed in the CPU system.

The most common VAX-11/780 CPU configuration supplied by DEC leaves an empty MBA slot between MBA slot zero and the Bus Terminator PCBA, as shown in Figures 4-12 and 4-13. This empty slot is MBA slot one.

If MBA slot one is not available, the V-MASTER/780 card cage assembly may be installed in the slot occupied by the standard DEC Bus Terminator PCBA. The DEC Bus Terminator PCBA is then replaced by an Emulex Bus Terminator PCBA that is installed on the backplane of the V-MASTER/780 card cage assembly (see subsection 3.8.5). When this installation method is used, an additional power supply is needed.

If the V-MASTER/780 card cage assembly is to be installed in DEC Expansion Box cabinet, ask an Emulex Technical Support representative for installation details (see subsection 5.3 for address, etc.).

4.5.5.1 V-MASTER in MBA Slot One

To install the V-MASTER/780 card cage assembly in MBA slot one of the VAX-11/780 CPU cabinet, use the following procedure:

a. Disconnect coaxial SBI bus cables that link SBI bus and empty DEC MBA card cage chassis.

b. Disconnect all power supply cables from empty DEC MBA card cage chassis, but leave power supply cables connected to power supply.

c. Remove four Phillips-head screws (two upper back and two lower front) that hold empty DEC MBA card cage chassis in place. Save screws.

d. Slide empty DEC MBA card cage chassis backwards out from rear of CPU cabinet.

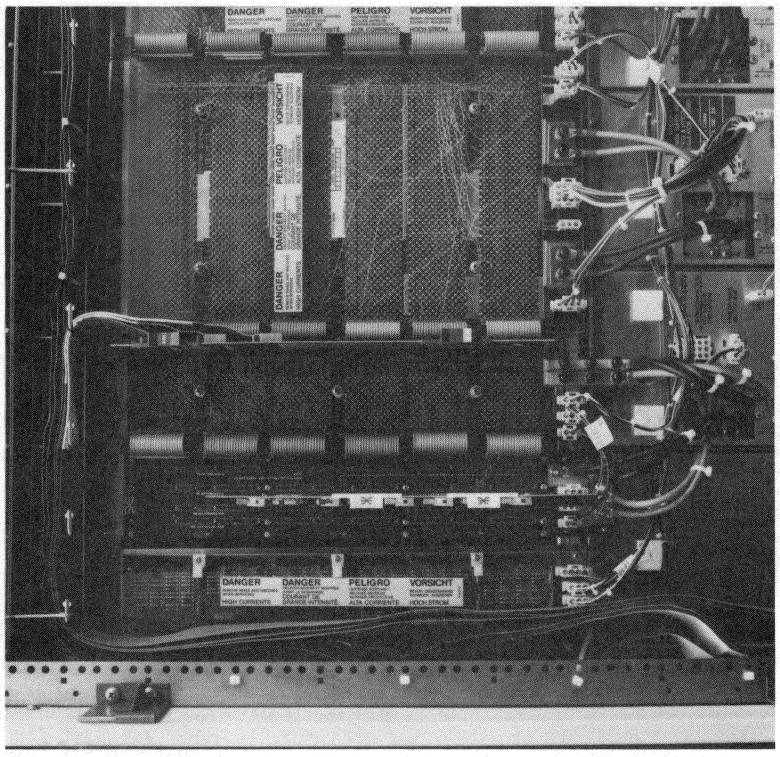


Figure 4-12. Single V-MASTER/780 Card Cage Installation

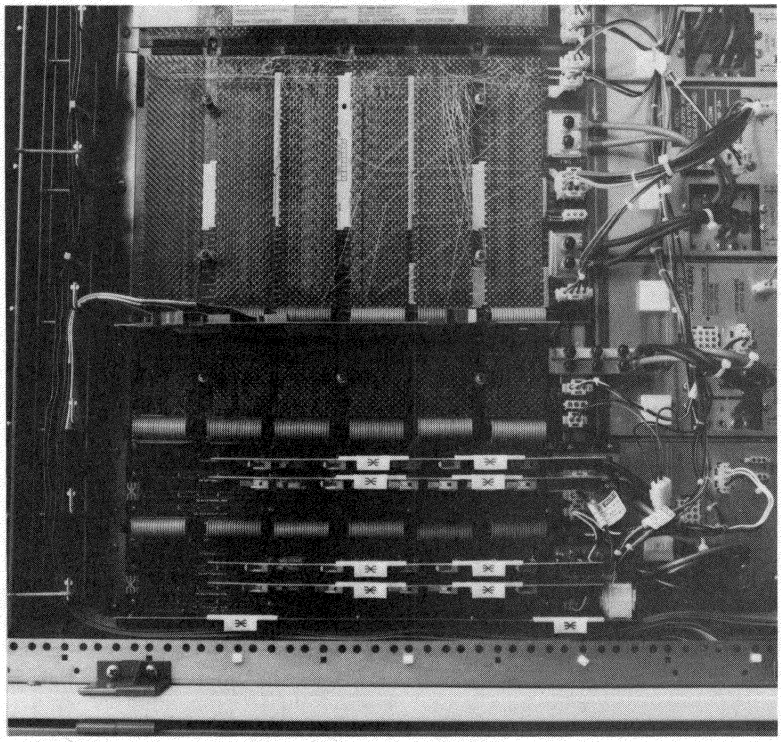


Figure 4-13. Dual V-MASTER/780 Card Cage Installation

e. Slide V-MASTER/780 card cage assembly from rear of CPU cabinet forward into MBA slot one position.

f. Secure V-MASTER/780 card cage assembly in place with four screws removed in step c.

g. Connect cables removed in steps a and b to V-MASTER/780 card cage assembly.

4.5.5.2 V-MASTER in Bus Terminator Slot

This installation requires an additional power supply. Two different versions are available from Emulex. Verify the correct version before replacing the dummy power supply with the Emulex power supply. Version -01 is used with a 120 Vac power source and version -02 is used with a 220 VAC power source. The version dash number follows the Emulex part number which is located on the rear side of the power supply near the Emulex logo. Connectors J3 through J7 are also located on the rear side of the power supply.

To install the V-MASTER/780 card cage assembly in the Bus Terminator slot, use the following procedure:

a. Disconnect coaxial SBI bus cables that link SBI bus and DEC SBI terminator assembly.

b. Disconnect all power supply cables from DEC SBI terminator assembly but leave power supply cables connected to power supply.

c. Remove four Phillips-head screws (two upper back, two lower front) that hold DEC SBI terminator assembly in place. Save screws.

d. Slide DEC SBI terminator assembly backwards out from CPU cabinet.

e. Slide V-MASTER/780 card cage assembly from rear of CPU cabinet forward into MBA slot formerly occupied by DEC SBI terminator.

f. Secure V-MASTER/780 card cage assembly in place with four Phillips-head screws removed in step c.

g. Connect SBI bus cable, disconnected in step a, to V-MASTER/780 card cage assembly.

h. Release clasp (rear, center bottom), on dummy power supply located at far left end of CPU cabinet (viewed from rear), by moving clasp toward right side of power supply.

i. Unscrew single Phillips-head screw (front, center top of dummy power supply) and slide dummy power supply out from front of CPU cabinet.

j. Install Emulex power supply in same location from which dummy power supply was removed by reversing steps h and i, then connect power supply cables to V-MASTER/780 card cage assembly. Connections should be made as shown in Figure 4-14.

4.6 BACKPLANE CABLING

The schematic of backplane cabling for VAX-11/780 CPUs is shown in Figure 4-14. The backplane cabling includes +5 VDC power cables, -5.2 Vdc power cables, AC/DC Low cables, and coaxial SBI bus cables.

4.6.1 +5 VDC POWER CABLES

Each V-MASTER/780 card cage assembly is connected to the appropriate power supply by four cables. These cables are American Wire Gauge (AWG) number eight. Two red cables are for the +5 Vdc side, and two black cables are for the ground side of the power supply. The +5 Vdc cables are run from the +5 VDC studs on the appropriate V-MASTER/780 backplane to the +5 VDC terminals on the power supply where they are attached with number 10 machine screws.

The ground cables are run from the ground (GND) studs on the appropriate V-MASTER/780 backplane to the ground terminals on the power supply where they are attached with number 10 machine screws.

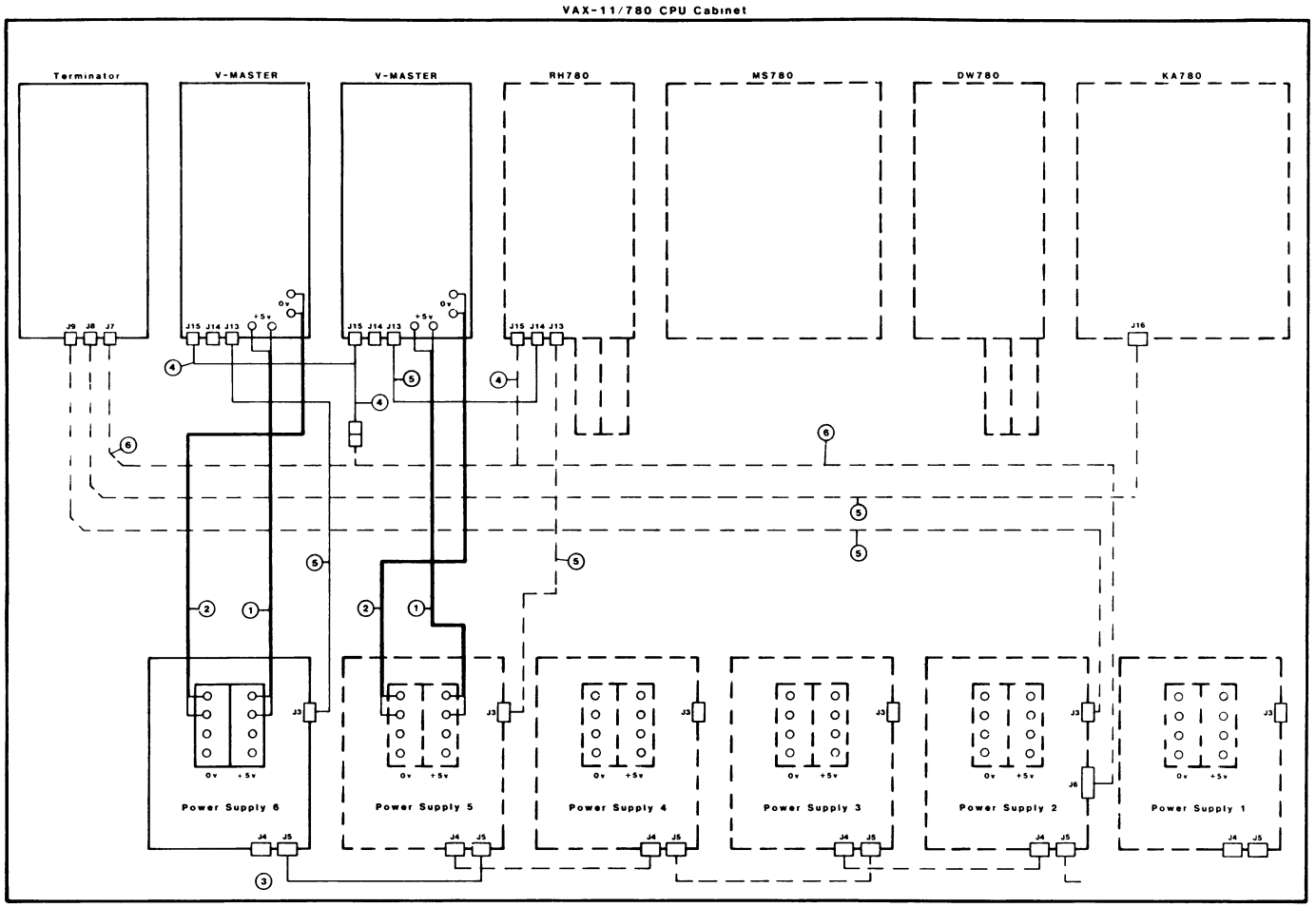
NOTE

The number 10 machine screws should already be in place on the power supply; however, spare screws are supplied with the V-MASTER/780 card cage assembly to enable connection if original screws are missing.

4.6.2 -5.2 VDC CABLE

The -5.2 Vdc cable runs from connector J6 on power supply two (second from left as viewed from rear of CPU cabinet) to the connector on the backplane of the CPU, from which a two-wire (blue-wire and black-wire) cable connector is connected to connector J15 on the V-MASTER/780 or to connector J15 on a DEC RH780 MBA. A jumper cable (Emulex P/N SU7811206) is included with the V-MASTER/780 card cage assembly so that a single connector can service two MBA backplane slots.

A combined +5 Vdc/-5.2 Vdc cable terminates at connector J7 of the SBI Bus Terminator PCBA.



Legend

No.	Description	Color
1	+ 5vDC	Red
2	0vDC	Black
3	Over Temp	Grey/White
4	-5.2vDC	Blue/Black
5	AC/DC Low	Yellow/Violet/Black
6	-5.2/5 vDC	Red/Black/Blue/Black

— — — DEC Harness and Hardware

——— Emulex Harness and Hardware

Figure 4-14. VAX-11/780 CPU Backplane Cabling Schematic

4.6.3 AC/DC LOW CABLES

The AC/DC Low cable is run from connector J3 of the power supply for the V-MASTER/780 or RH780 MBA to connector J13 on the backplane for the V-MASTER/780 or RH780 MBA. If more than one V-MASTER/780 or RH780 MBA is serviced by the power supply, the second unit receives AC/DC Low signal via a jumper from connector J14 on the first unit to connector J13 on the second unit.

A second set of two AC/DC Low cables form a loop from connector J3 of the second power supply to connector J9 of the SBI Bus Terminator and then returns from connector J8 of the SBI Bus Terminator to connector J16 of the DEC KA780 CPU module backplane.

4.6.4 COAXIAL SBI BUS CABLES

Each chassis in the VAX-11/780 CPU cabinet is linked by six coaxial cables that carry the SBI bus signals. These cables originate at connectors J1 through J6 on the left edge of each chassis and terminate at connectors J7 through J12, respectively, on the right edge of each chassis. The header for each coaxial SBI Bus cable is self-aligning, to ensure no pins are bent when the header is installed. As part of this feature, however, each header does allow a pair of pins to be open above or below the header, or an entire row of pins to the left or right of the header to be missed -- without equipment damage.

After pressing each header into proper position, and before system power up, use a flashlight or equivalent bright illumination, and carefully inspect each header to verify proper installation has been done.

4.7 CABLE ROUTING AND RFI SUPPRESSION

Figure 4-15 is a schematic of tape transport cable routing. Limits for RFI are governed by requirements of the Federal Communications Commission (FCC). This subsection describes the features, use, and installation of the RFI-suppression devices, manufactured by Emulex Corporation, to meet the following FCC requirements:

> "This device is a subassembly in the context of Subpart J of Part 15 of FCC Rules. It has been tested in typical packaging and normal usage, and under these conditions, operates within the limitations of Class 'A' equipment.

Excerpt from FCC 83-352 33659 Docket 80-284:

> "Where special accessories, such as shielded cables, are required in order to meet FCC emissions limits, appropriate instructions on the need to use such equipment must be contained in the user manual."

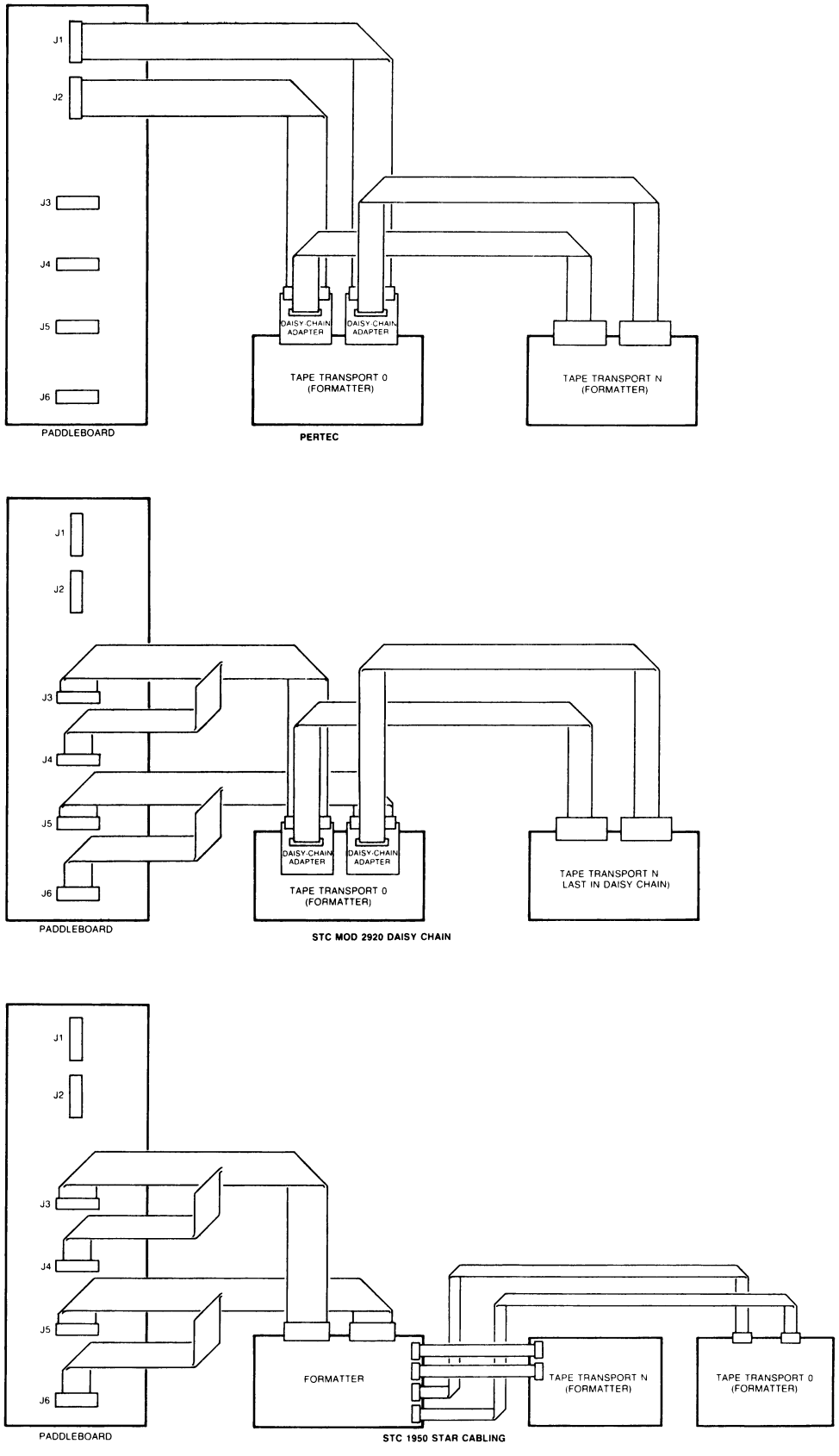


Figure 4-15. Tape Transport Cabling Schematic

4.7.1 EQUIPMENT CABINET

The equipment cabinet in which the computer equipment is installed should be a standard 19-inch wide EIA or RETMA equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free from holes, except small perforations for air exhaust are permitted.

New equipment cabinets for DEC systems have a specially fabricated rear bulkhead door or panel in which apertures have been cut. These apertures are designed for installation of blank panels or panels with slots and associated grounding bars to provide feed-through shield grounding for cables that connect equipment mounted within the cabinet and equipment mounted in other cabinets. All such apertures must be filled with one of these panels. These panels are called "Personality Panels" and are all the same size, as shown in Figure 4-16.

4.7.1.1 Same Cabinet

If the TC7000 Tape Coupler PCBA or V-MASTER/780 card cage assembly with TC7000 Tape Coupler PCBA is mounted in the same cabinet as the CPU, the main concern is installing the system so that no gaps are left in the shield. The rear of the CPU cabinet is typically shielded with a bulkhead from top to bottom. The bulkhead is segmented to ease installation of different optional peripheral devices. Each segment has two apertures, each of which is covered by a blank panel. The general procedure is to remove one of the blank panels from the bulkhead segment and replace that blank panel with a Personality Panel (Emulex P/N TU1210201), or to remove the entire bulkhead segment and replace it with a Bulkhead Distribution Panel (Emulex P/N CU2220301). To maintain the integrity of the RFI shield, there must be no gap above or below the replacement panel after that panel is installed. If continuity of shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

4.7.1.2 Separate Cabinets

If the TC7000 Tape Coupler PCBA or V-MASTER/780 card cage assembly with TC7000 Tape Coupler PCBA is mounted in a separate cabinet from that of the CPU, that expansion cabinet must prevent RFI radiation by being shielded in the same way the DEC CPU cabinet is shielded. Also, the cable that connects to the CMI or VMI in the CPU cabinet must be shielded, since it is external to the shielded cabinet environment.

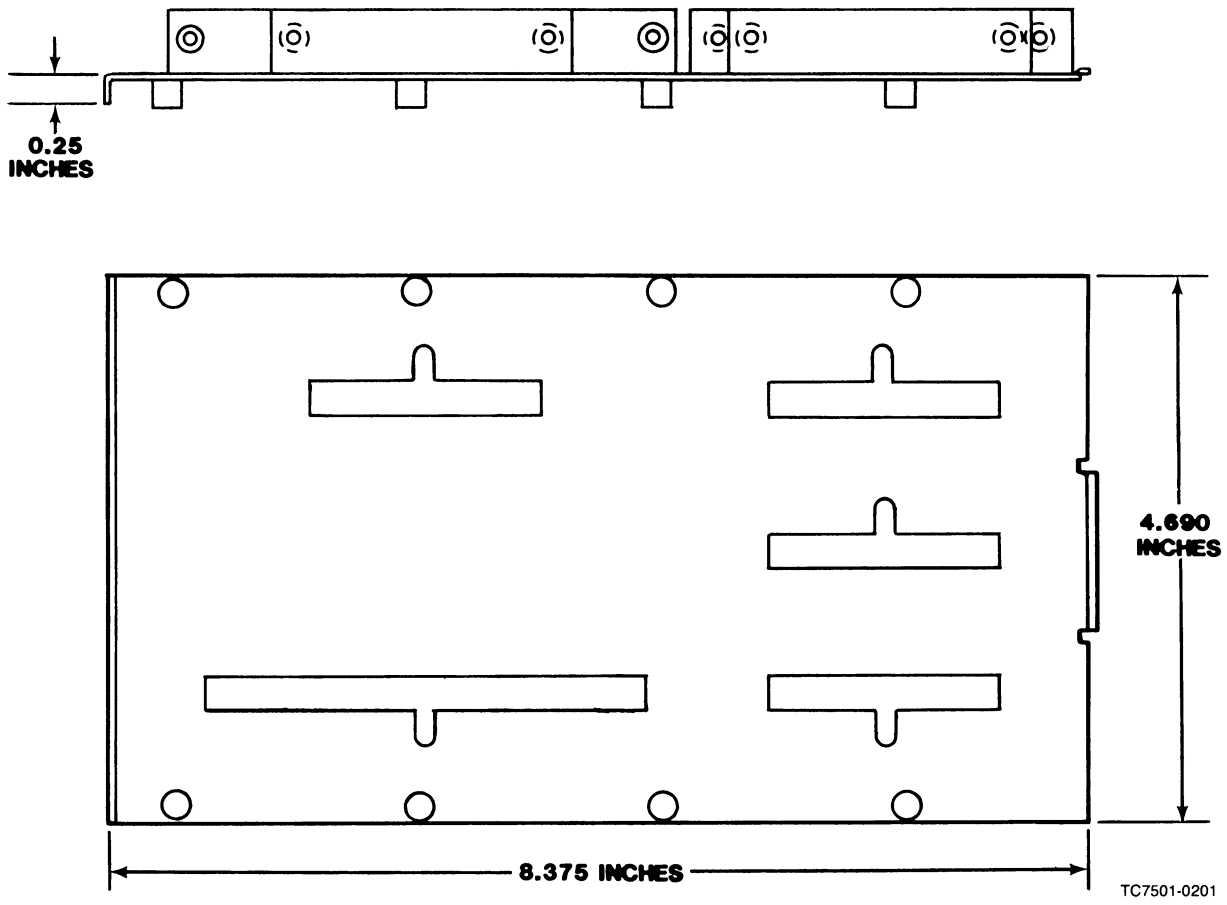


Figure 4-16. Personality Panel Dimensions

For installation of related tape transports in separate cabinets, Emulex recommends using a hardened cabinet such as the Everest Electronic Equipment Model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full-length, segmented bulkhead in the rear. One of the segments should be removed and replaced with a Bulkhead Distribution Panel or with a rack-mount panel that contains a blank panel and a Personality Panel (these components are needed to allow the shielded cable from the TC7000 Tape Coupler to be terminated). As in the DEC cabinet, there must be no gap above or below any rack-mounted panel when the installation is complete.

To prevent the introduction of conducted interference on the ac line that feeds the internal power supply, a power distribution panel with a line filter must be installed in the expansion cabinet. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated.

4.7.1.3 Shielding

For older equipment-cabinet installations that lack complete metal shielding, all system cabling inside and outside the cabinet must be shielded. For new equipment cabinets that provide complete shielding, only those cables that run outside the cabinet(s) must be shielded.

4.7.1.4 Grounding

Ground returns and shielding of all cabling within the rack/cabinet must be grounded to the cabinet, and the cabinet itself must have a sure Earth ground. All cable ground returns and shielding entering the cabinet must be properly grounded, once inside the cabinet.

4.7.2 RFI-SUPPRESSION DEVICES

The RFI-suppression devices developed by Emulex consists of suitable Personality Panels, unshielded cables for connections within the equipment cabinet, and shielded/jacketed cables that are routed between the cabinets. Two Personality Panels are required; one for each end of the shielded/jacketed cable(s). The Personality Panel for tape controllers and tape couplers is Emulex P/N TU1210201.

For older equipment cabinets that lack the bulkhead with apertures for blank panels and Personality Panels, Emulex provides a special bulkhead distribution panel (Emulex P/N CU2220301) that can be mounted on the back of an equipment cabinet. Mounting requires four screws on each end, as shown in Figure 4-17. This distribution panel has apertures for the blank panels and Personality Panels.

Cable details for the tape controllers and tape couplers are listed in Table 4-5 with lengths in feet (ft) or inches (in.), as applicable.

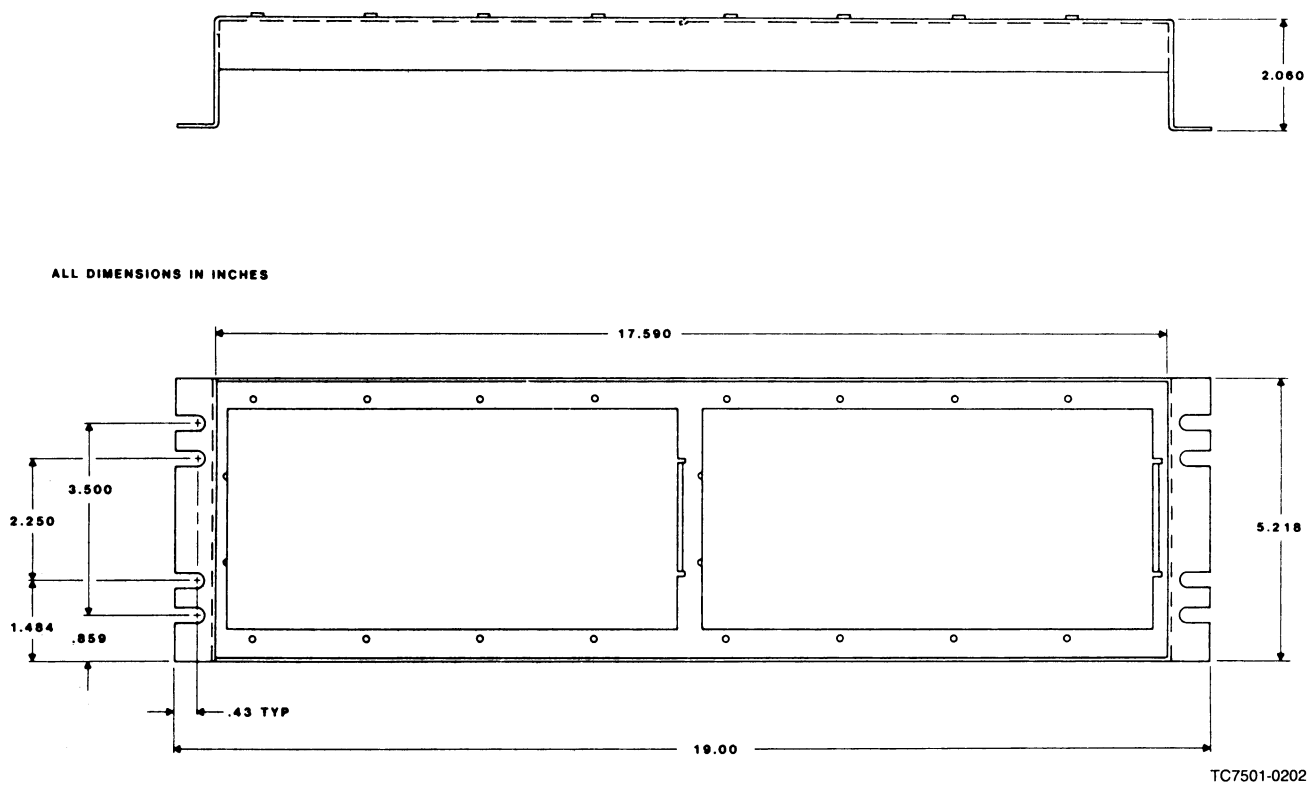


Figure 4-17. CU2220301 Bulkhead Distribution Panel

CAUTION

Maximum cable length, including ALL daisy-chain cables, must be not more than 20 feet for any interface.

Table 4-5. Shielded Cables and Installation Hardware

Item	Part Number	Description	Qty Rqd	Interface
1	SU7811212-01	Cable, Shielded, 4 ft	2	STC
	SU7811212-02	Cable, Shielded, 8 ft	2	STC
	SU7811212-03	Cable, Shielded, 15 ft	2	STC
2	SU7511201-01	Cable, Unshielded, 15 ft	2	STC
3	SU7811219-01	Cable, Unshielded, 2 ft	2	STC
	SU7811219-02	Cable, Unshielded, 4 ft	2	STC
	SU7811219-03	Cable, Unshielded, 6 ft	2	STC
	SU7811219-04	Cable, Unshielded, 8 ft	2	STC
	SU7811219-05	Cable, Unshielded, 10 ft	2	STC
4	TU1211202-01	Cable, Shielded, 3 ft	2	Pertec
	TU1211202-02	Cable, Shielded, 5 ft	2	Pertec
	TU1211202-03	Cable, Shielded, 8 ft	2	Pertec
	TU1211202-04	Cable, Shielded, 15 ft	2	Pertec
5	TU1211204-01	Cable, Unshielded, 20 in.	2	Pertec
	TU1211204-02	Cable, Unshielded, 40 in.	2	Pertec
	TU1211204-03	Cable, Unshielded, 60 in.	2	Pertec
	TU1211204-04	Cable, Unshielded, 80 in.	2	Pertec
	TU1211204-05	Cable, Unshielded, 100 in.	2	Pertec
	TU1211204-06	Cable, Unshielded, 120 in.	2	Pertec
6	TU1211203-01	Cable, Unshielded, 20 in.	2	Pertec
	TU1211203-02	Cable, Unshielded, 40 in.	2	Pertec
	TU1211203-03	Cable, Unshielded, 60 in.	2	Pertec
	TU1211203-04	Cable, Unshielded, 80 in.	2	Pertec
	TU1211203-05	Cable, Unshielded, 100 in.	2	Pertec
	TU1211203-06	Cable, Unshielded, 120 in.	2	Pertec
7	TU1210201	Personality Panel	2	All
8	CU2220301	Bulkhead Distribution Panel (optional)	2	All

The items listed in Table 4-5 can be ordered from your Emulex sales representative or directly from the factory. The factory address is:

Emulex Customer Service
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

4.7.3 CABLE INSTALLATION

Most Emulex products are installed directly in the backplane of a CPU or expansion box manufactured by DEC. If the cabinet which houses the CPU or expansion box has enough room to include the peripheral(s) controlled by the Emulex product, those peripherals should be housed in the same cabinet. In such an installation, no shielded interconnect cables are required because the equipment cabinet itself provides the shielding. If the cabinet is the older type which does not provide complete shielding, the cables between the Emulex product and the interconnected equipment must be shielded, even when the cables are not routed outside the cabinet.

When peripherals controlled by the Emulex product(s) are not housed in the same equipment cabinet, the equipment must be interconnected by suitable RFI-suppression devices that ground all shielded cables entering the equipment cabinet.

To install the Emulex RFI-suppression devices, see Figure 4-16 and 4-18 and use the following procedure:

a. Open rear bulkhead door or panel of CPU equipment cabinet.

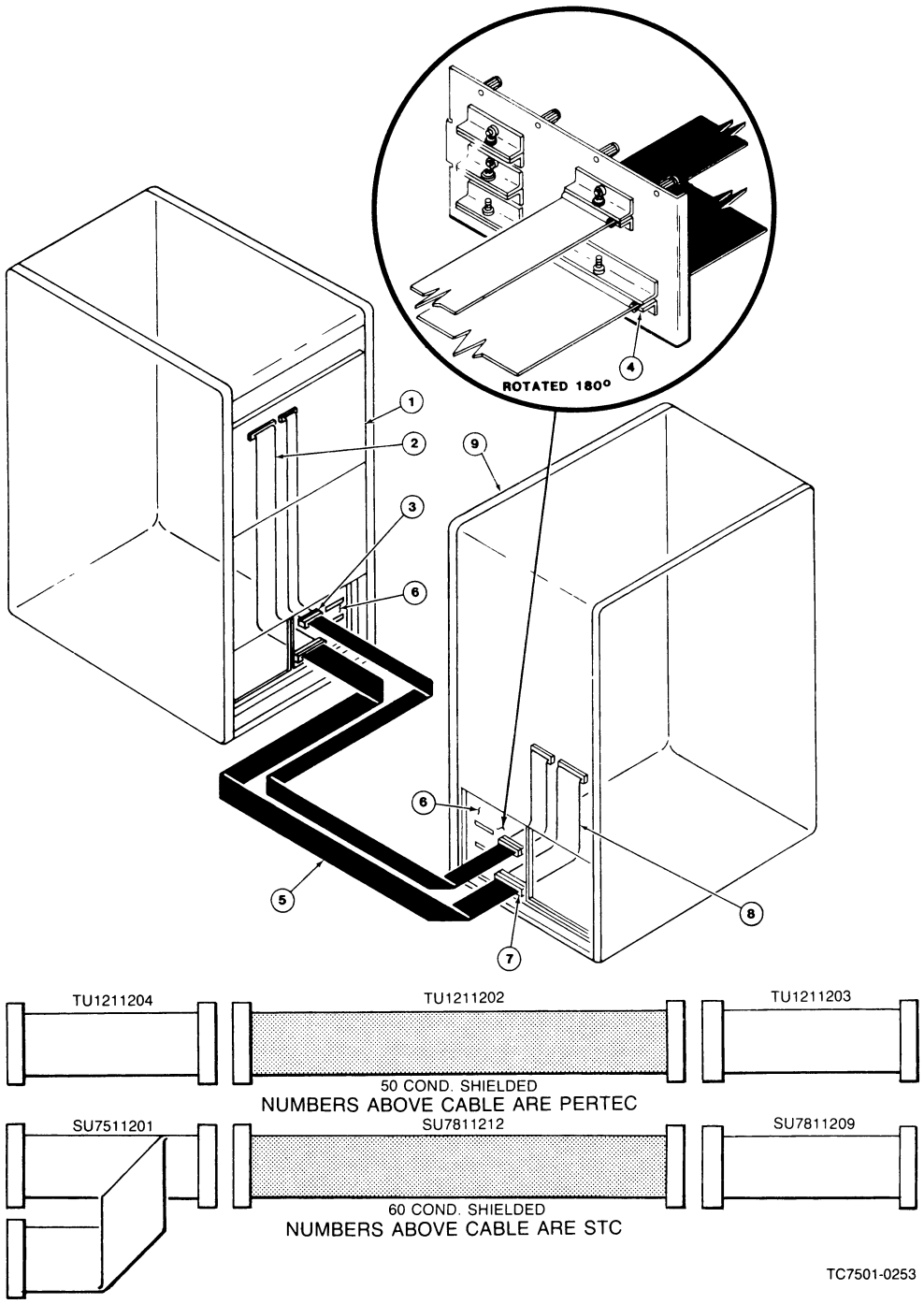
b. Install Emulex TC7000 Tape Coupler or V-MASTER/780 card cage in appropriate CPU bus slots (see subsection 4.4.7 or 4.5.5, as applicable).

c. Install appropriate Personality Panel in convenient aperture in rear bulkhead of equipment cabinet for TC7000 Tape Coupler and secure in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panel.

d. Install two Personality Panels in convenient aperture in rear bulkhead of equipment cabinet for first tape transport in daisy chain and secure each in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panels.

e. Repeat step d for cable entry to and exit from cabinets for remaining tape transports to be in daisy chain.

f. Select shielded interface cable [P/N SU7811212 (60-pin) or TU1211202 (50-pin), as applicable] long enough to reach from Personality Panel for TC7000 Tape Coupler to Personality Panel for cable entry to first tape transport.



1. TC7000 TAPE COUPLER PCBAs
2. NONSHIELDED EXTENSION CABLE, TC7000 TAPE COUPLER - SHIELDED CABLE
3. CABLE CONNECTORS, TC7000 TAPE COUPLER - SHIELDED CABLE
4. CLAMP - SHIELD OF SHIELDED CABLE CLAMPED WITHIN
5. SHIELDED/JACKETED CABLE, EXTERNAL TO EQUIPMENT CABINETS
6. PERSONALITY PANELS
7. CABLE CONNECTORS, SHIELDED CABLE - TAPE TRANSPORT(S)
8. NONSHIELDED EXTENSION CABLE, SHIELDED CABLE-TAPE TRANSPORT
9. TAPE TRANSPORT

Figure 4-18. RFI-Suppression Cable Installation

g. Strip about one inch of shielded insulation from end of cable for TC7000 Tape Coupler to expose shield. Cut shield at each edge to allow shield to be folded back over insulation, then fold shield over insulation. Route prepared cable ends through appropriate slots in Personality Panel and clamp exposed shielding securely in Personality Panel (see detail in Figure 4-18). Repeat this process at other end of cable.

h. Select unshielded interface cable [P/N SU7811215 (60-pin) or TU1211204 (50-pin), as applicable] long enough to reach from Cable Paddleboard PCBA to associated Personality Panel in cabinet bulkhead.

i. Find arrow molded into header of cable connector for mating Cable Paddleboard PCBA connector (J1 or J2 Pertec, or J3 through J6 STC, as applicable). Arrow identifies pin 1 of connector.

j. Find arrow molded into header of mating Cable Paddleboard connector, then align arrows and connect mating connectors.

k. Repeat steps i and j for other cable connections at Cable Paddleboard PCBA.

l. Find arrow molded into header of cable connector that mates with connector on shielded cable in Personality Panel. Arrow identifies pin 1 of connector.

m. Find arrow molded into header of mating shielded cable connector, then align arrows and connect mating connectors.

n. Repeat steps l and m for other cable connections at Personality Panel for TC7000 Tape Coupler.

o. Select unshielded interface cable [P/N SU7811219 (60-pin) or TU1211203 (50-pin), as applicable] long enough to reach from connector on formatter for tape transport to associated Personality Panel in rear bulkhead of tape transport cabinet.

p. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.

q. Interconnect tape transports to be daisy chained as instructed in tape transport technical manual. Verify last tape transport in daisy chain is properly terminated. If tape transports are in separate extension cabinets, use shielded cable between cabinets as described in foregoing steps of this procedure.

r. Close bulkhead door or panel on each equipment cabinet.

s. Turn system power ON.

4.7.4 SYSTEM INTERCONNECTIONS

Subsystem cabling for the TC7000 Tape Coupler and tape transport interface is different for Pertec and STC units. Cabling for daisy chaining eight Pertec tape transports to the Cable Paddleboard PCBA is shown in Figure 4-19. Cabling for daisy chaining four STC tape transports to the Cable Paddleboard PCBA is shown in Figure 4-20.

NOTE

Flat cable connectors on the Cable Paddleboard PCBA and on the I/O cables are not keyed, and can be inadvertently reversed. No damage should result from reversed cable connection, but the subsystem cannot function. The connectors on each cable have an arrowhead moulded into the connector body next to pin 1. The arrowhead can be seen and felt. On the Cable Paddleboard PCBA, pin 1 of each connection is in the front left corner.

At the first tape transport, the I/O cables are connected to connectors on the tape transport as instructed in the tape transport technical manual. Each tape transport in the daisy chain must be interconnected to the preceding tape transport in the same way the Cable Paddleboard PCBA for the TC7000 Tape Coupler is connected to the first tape transport.

NOTE

Not all tape transport models have two sets of one-to-one interconnected connectors to ease daisy chaining. Tape transports which lack paired connectors must use I/O cables with paired connectors.

Only the last tape transport in a daisy chain must be terminated. Termination is made by installing one or more terminator resistor modules. Such termination assemblies are supplied by the tape transport manufacturer as part of the tape transport. To install the terminator assemblies, see the tape transport technical manual. Terminator details are provided in Appendix B.

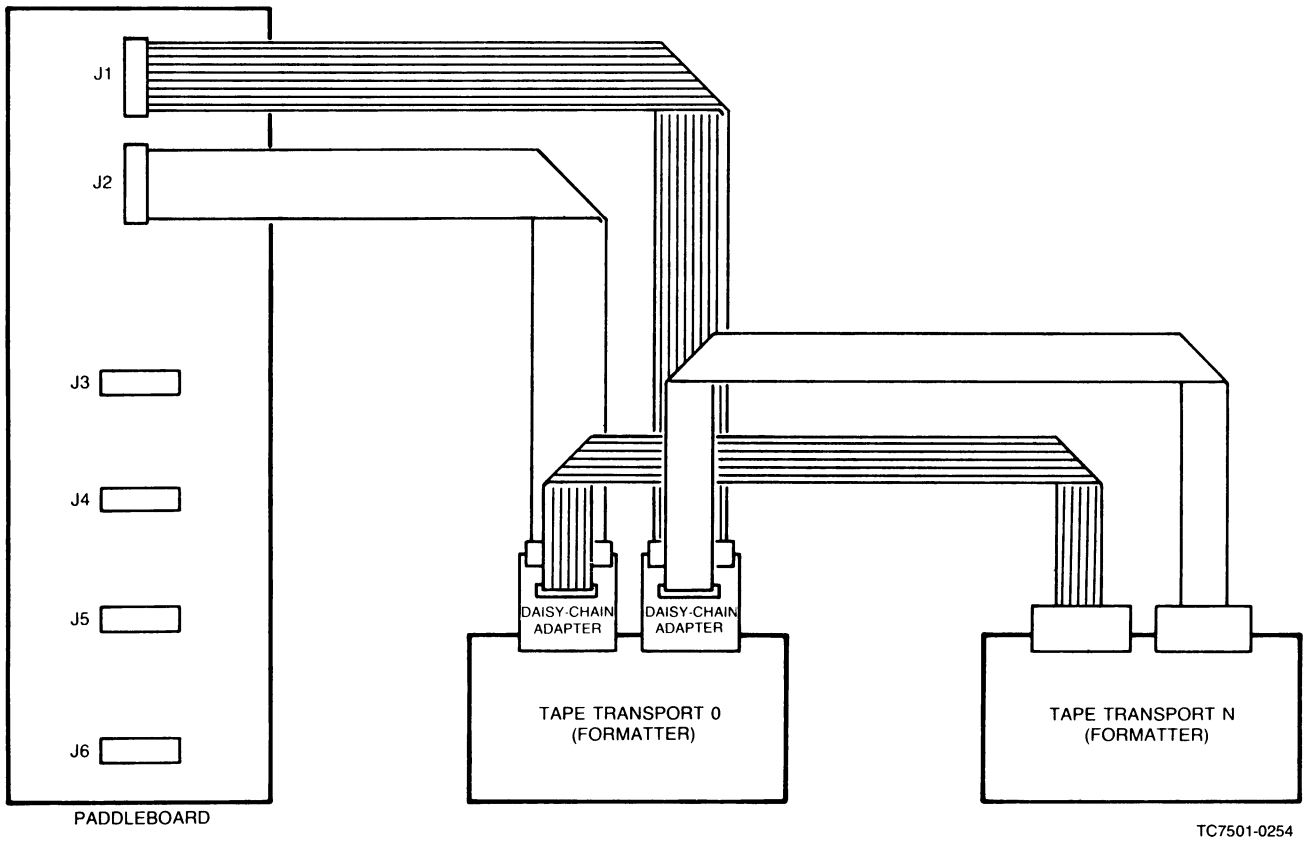


Figure 4-19. Daisy Chaining Pertec Tape Transports

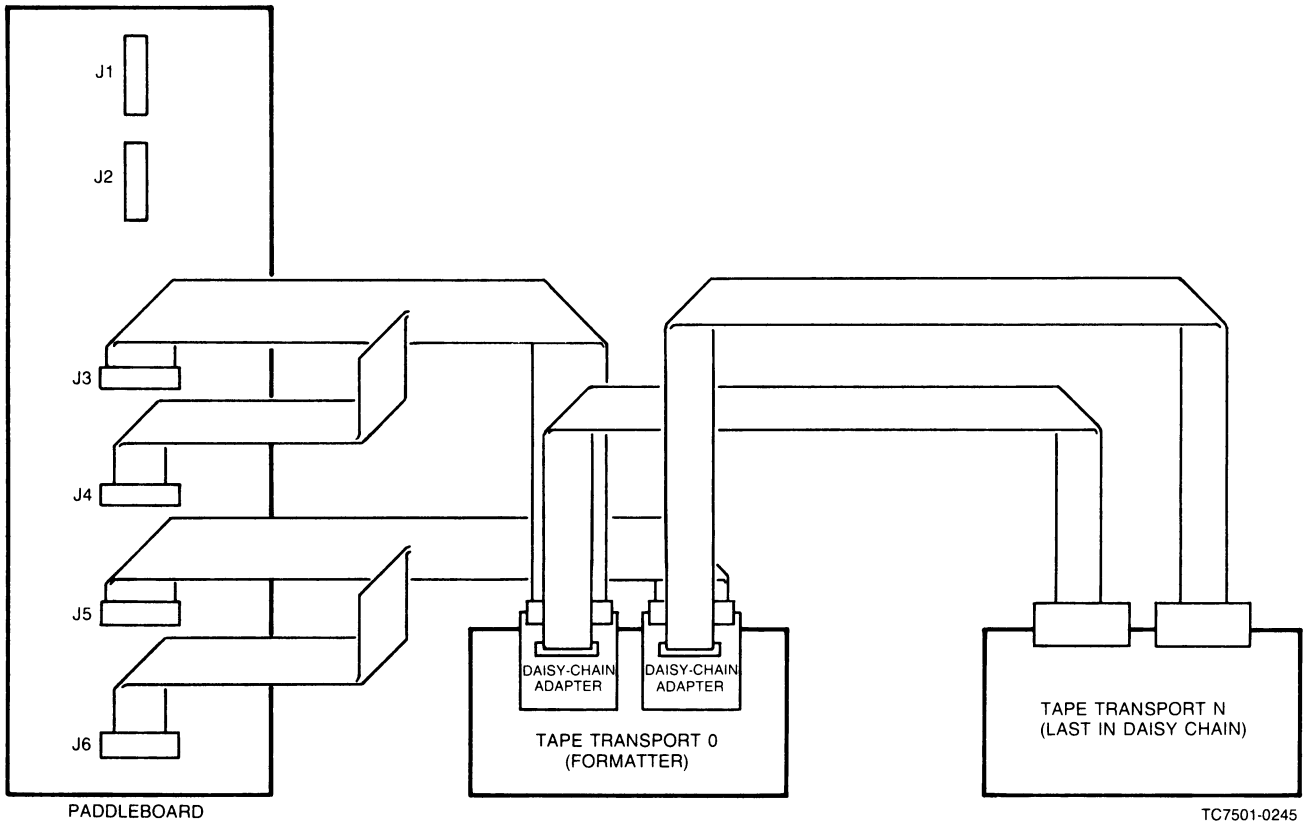


Figure 4-20. Daisy Chaining STC MOD2920 Tape Transports

4.7.4.1 Pertec I/O Cabling

Connectors J1 and J2 on the Cable Paddleboard PCBA are used to connect the I/O cables between the TC7000 Tape Coupler and the first Pertec-type tape transport in the system. The tape transports used need not be Pertec units, but they must be compatible with the Pertec interface. Some examples of tape transports that have Pertec interface are models manufactured by Control Data Corporation (CDC), Kennedy, and Cipher Data Products, Inc.

4.7.4.2 STC I/O Cabling

Connectors J3, J4, J5 and J6 on the Cable Paddleboard PCBA are used to connect the I/O cables between the TC7000 Tape Coupler and the STC tape formatter. The STC model 1935 formatter has separate cable sets that interface with up to four STC model 1950 tape transports. Connectors J3/J4 of the cable set are connected to the A4 connector on the STC formatter. Connectors J5/J6 of the cable set are connected to the B4 connector on the STC formatter (see Appendix B).

4.7.5 GROUND STRAP

For proper operation of the computer system, all components must have a good chassis ground. This ground connection should be 1/4-inch braid (preferably insulated) or AWG number 10 (or larger) wire. The grounding wire may be daisy-chained between the tape transports.

NOTE

Failure to observe proper grounding methods generally results in marginal system operation with random error conditions.

4.8 TESTING

Testing involves self-test, register examination, and diagnostics.

4.8.1 SELF-TEST

When power is applied to the CPU, the TC7000 Tape Coupler automatically executes a built-in self test. This self-test routine is not executed every time an INIT signal is detected on the VMI (or CMI) Bus, but only when the CPU is powered up. If the self test is successfully executed, the FAULT LED on the front edge of the TC7000 Tape Coupler should be extinguished. A flashing FAULT LED indicates successful Self-Test but tape transport(s) are not connected to the system, or if connected are not in the On-Line mode. Steady illumination of the FAULT LED indicates unsuccessful Self-Test execution, and that the TC7000 Tape Coupler cannot be addressed by the CPU.

4.8.2 REGISTER EXAMINATION

After the CPU is powered up and the FAULT LED on the TC7000 Tape Coupler is not lit, a quick check should be made to ensure the registers on the TC7000 Tape Coupler can be read. The device status register (TMDS) should have bits 01 and 12 set if the tape transport is on line and the tape is loaded at the Beginning of Tape (BOT) marker.

4.8.3 DIAGNOSTICS

The TC7000 Tape Coupler executes the following diagnostics:

EVMAA - Data Reliability

EVMAC - Control Logic Test.

On the EVMAC Control Logic Diagnostic Test, only Tests 1 through 8 and 23 through 27 are run because the other tests use internal maintenance functions in the TM03 Formatter which are not supported by the TC7000 Tape Coupler.

NOTE

EVMAA and EVMAC both have tests which make use of the read reverse feature in GCR mode. Thus, these diagnostics will only run in PE mode on drives (such as the CDC 92185) which do not support read reverse.

5.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the TC7000 Tape Coupler system. This section is divided into four subsections, as listed in the following table:

Subsection	Title
5.1	Overview
5.2	Preventive Maintenance
5.3	Service
5.4	Fault Isolation

5.2 PREVENTIVE MAINTENANCE

The regularly scheduled maintenance checks, cleaning procedures, component replacement procedures and adjustment procedures detailed in the separately supplied system component technical manuals should be accomplished at the prescribed intervals. There are no adjustments or calibrations required in servicing the TC7000 Tape Coupler. Emulex recommends the diagnostic software programs be used in the system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circuit component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

Preventive maintenance of the TC7000 Tape Coupler system also includes three periodic verifications:

a. Proper seating of TC7000 Tape Coupler PCBAs in CPU backplane, or in V-MASTER/780 card cage assembly, as applicable.

b. Proper seating of cables in connectors.

c. Proper seating of PROMs in their respective IC sockets.

These verifications should be made about once a year or whenever physical location of components of the TC7000 Tape Coupler system is changed.

5.3 SERVICE

The components of the Emulex TC7000 Tape Coupler have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory. Except for setting DIP switches and placing jumpers on proper connective points (see Appendix B), no adjustments or alignments are required. If a malfunction does occur, as indicated by Fault Isolation procedures, and a component is not working properly, the entire TC7000 Tape Coupler should be returned to the factory or to an Emulex-authorized repair center for service. Emulex products are not designed to be repaired in the field.

5.3.1 EXPEDITING

If the TC7000 Tape Coupler is to be returned, Emulex recommends that a description of the symptoms and operating environment be included with the returned unit to expedite troubleshooting. Figure 5-1 shows a configuration record sheet to be filled in. The depicted configuration shows component locations, PROMs, DIP switch settings and cable connections.

Before returning the TC7000 Tape Coupler to Emulex, whether it is or is not under warranty, request the factory or the factory representative to provide return-shipment instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A PRODUCT OR COMPONENT TO EMULEX WITHOUT AUTHORIZATION

A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii notify:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

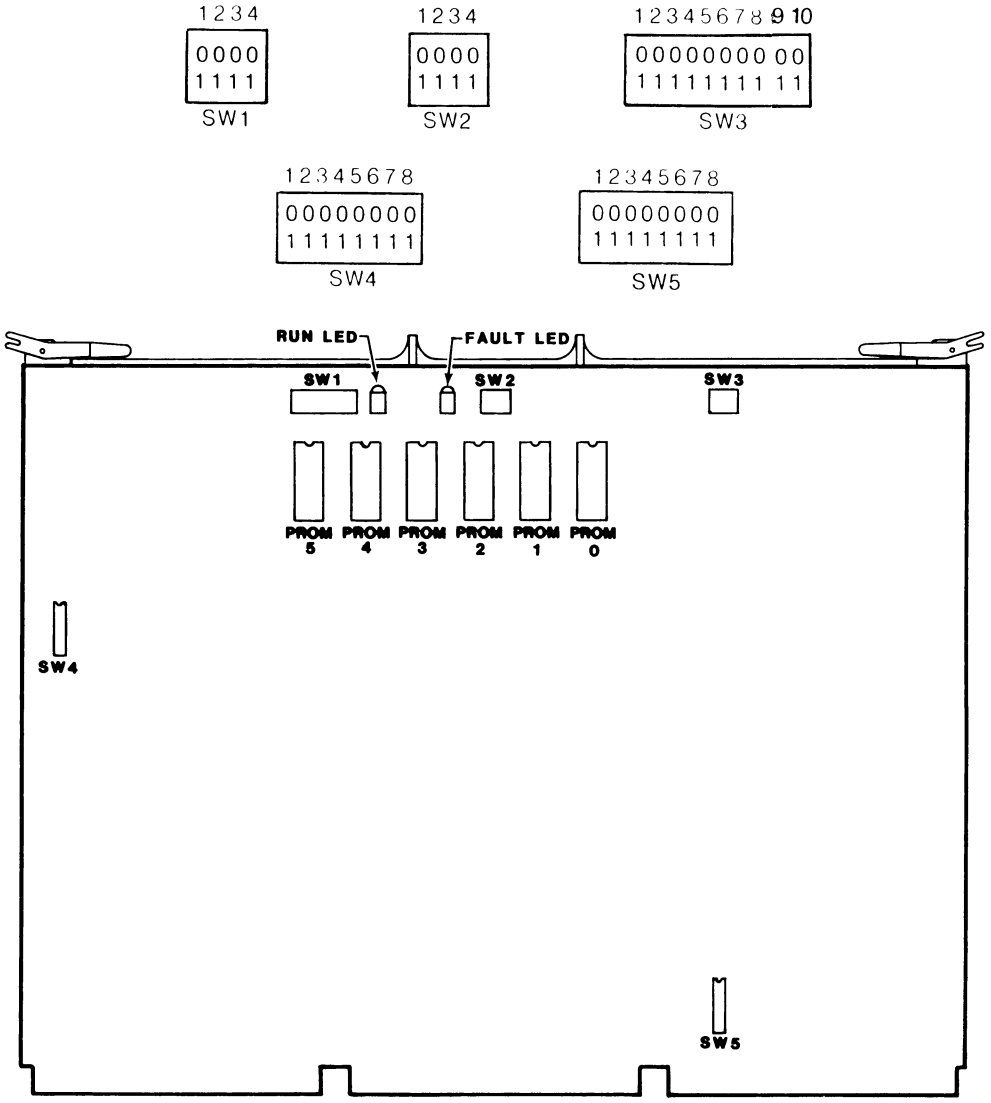
Outside the United States, notify the distributor from whom the product or component was initially purchased.

After notifying Emulex and receiving an RMA, package the product (preferably by using the original packing material) and send the product **POSTAGE PAID** to the address provided by the Emulex representative. The sender must also insure the package.

TC7000 CONFIGURATION RECORD SHEET

1. Emulation PROM numbers range from _____ to _____

2. Switch settings (circle 1 or 0)



Tape Coupler PCBA

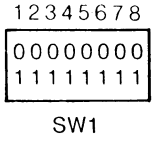
Use Pencil

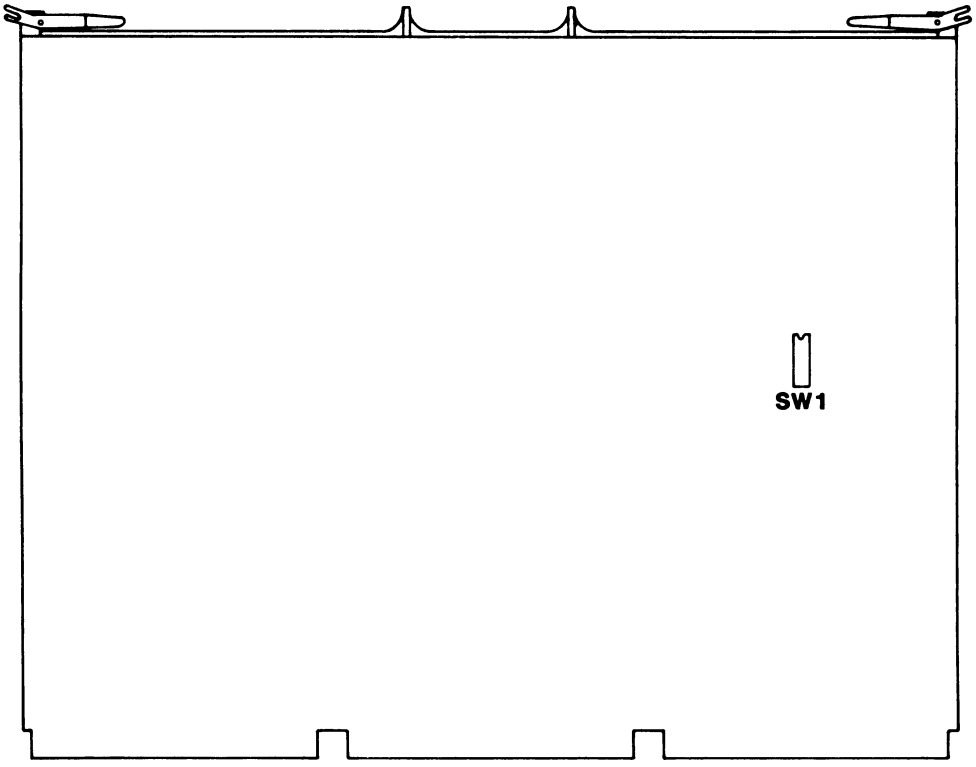
TC7501-0255

Figure 5-1. Configuration Record Sheet (SH 1 of 3)

1. Emulation PROM numbers range from _____ to _____

2. Switch settings (circle 1 or 0)





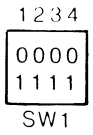
Bus Interface PCBA

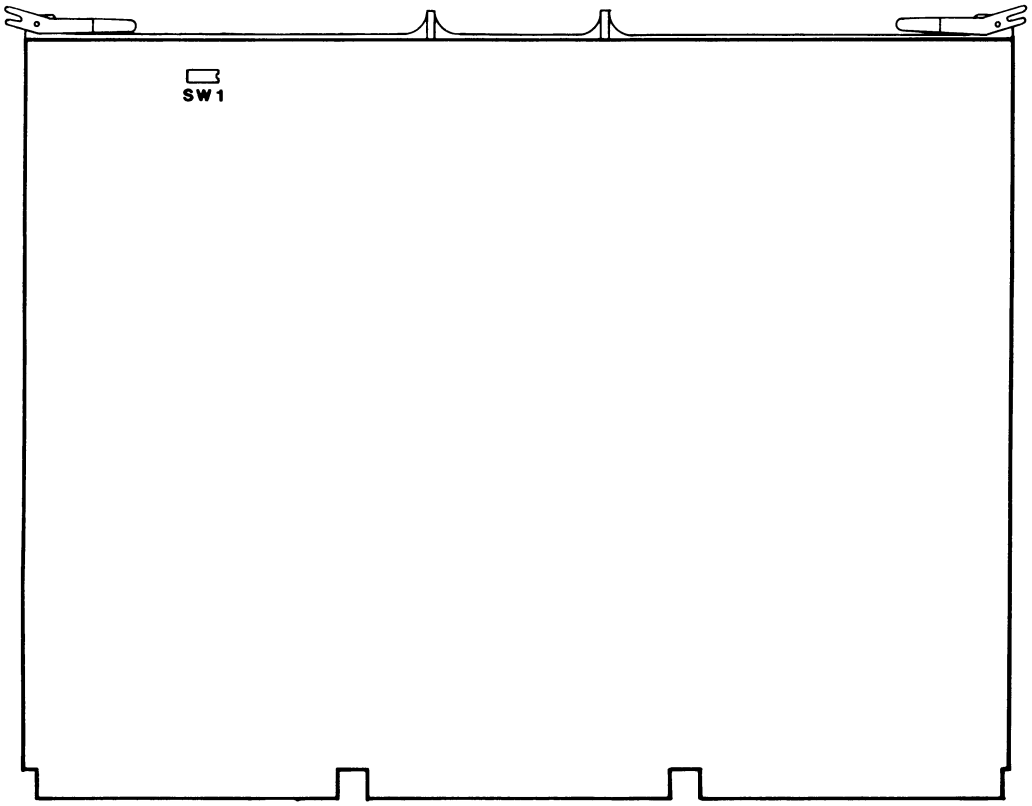
Use Pencil

Figure 5-1. Configuration Record Sheet (SH 2 of 3)

1. Emulation PROM numbers range from _____ to _____

2. Switch settings (circle 1 or 0)





Bus Translator PCBA

Use Pencil

Figure 5-1. Configuration Record Sheet (SH 3 of 3)

5.4 FAULT ISOLATION

The ensuing suggested fault isolation procedures are general in nature, based on established troubleshooting techniques, and should be used primarily as a guide. Following these procedures can aid in determining whether the equipment failure is a result of operator error or equipment malfunctions, speed location of a failed circuit component, and minimize down time caused by equipment malfunctions.

5.4.1 ISOLATING THE PROBLEM

In troubleshooting electronic equipment, the problem can usually be attributed to any of three sources:

a. Operator error

b. Adverse environmental factor(s)

c. Equipment malfunction.

Operator error is a more prevalent source of equipment problems than most operators care to admit. Operating procedures should always be investigated and eliminated **BEFORE** assuming any other source of malfunction exists. The symptoms should not be systematically investigated for environmental or electromechanical symptoms of malfunction until all possibility of human error has been eliminated.

5.4.2 OPERATING PROCEDURE CHECK

A system malfunction, appearing to be caused by circuit failure, is often found to be the result of improper operation or application of the equipment. When a problem is observed, the operating procedures being used with the malfunctioning unit and its associated units must therefore be thoroughly checked to ensure they are being correctly performed.

5.4.3 MANUAL OPERATIONS CHECK

A check must be made to determine if manual operations such as cleaning, servicing, or troubleshooting were performed on the equipment or related equipment before the first observed abnormal operation. Recently performed manual operations are suspect and should be double-checked to ensure that they were properly executed. Emulex recommends the following checks:

a. Verify recently changed procedures correctly performed

b. Verify adjustment settings properly made

c. Verify tightness of system connector installations

d. Verify that any parts temporarily removed or disconnected were properly and securely replaced; this check should

include proper seating of PCBAs in slots of V-MASTER/780 card cage, or CPU backplane.

e. Verify that no accidentally loosened or damaged components are evident. Tighten any loose components and replace any obviously damaged components.

5.4.4 VISUAL INDICATOR CHECK

If the malfunction persists after double-checking all recent manual operations, visually check the status of all operating controls and indicators in the system. Visual indicators include the following items:

a. Switches and indicator lights on PCBAs and operator control panels (OCPs)

b. Busses

c. Switches and/or indicators mounted out of sight on internal chassis or PCBAs

d. Printed data outputs

e. Signals monitored at test points by using meters, oscilloscopes, etc.

Correct any observed control-setting errors. Attempt to determine possible causes of erroneous indication.

5.4.5 POWER CIRCUIT CHECK

The effects of power supply malfunctions are normally widespread, which makes diagnosis of the problem difficult. Error indications tend to appear throughout the equipment and are difficult to localize. These symptoms, however, can sometimes be used as an indication that the cause of the problem is basic and pertains to the power circuits.

5.4.5.1 Fuses

Verify that all fuses in the power circuits are of the proper type and rating, and that none have blown. This check should include any fuses (or circuit breakers) internally mounted and not readily accessible from the front or rear of the major units of the system. Remove any blown fuse and replace with new fuse of the same type and rating.

CAUTION

Fuses with higher ratings or faster blow time limits than those removed must **NEVER** be installed. Determine cause of fuse failure and correct problem **BEFORE** replacing failed fuse.

5.4.5.2 Voltage Levels

Verify that power of the proper frequency and amplitude is being supplied to the equipment. If the primary input power is correct, check the output levels from all internal power supplies. All such outputs must be within required specifications (see applicable technical manuals for the equipment) and not subject to slow or intermittent drifting. If the problem is cyclic or intermittent; i.e., appears for a period of time and then disappears, check the power supplies for extreme sensitivity to variations in ambient temperature (heat or cold).

5.4.6 ELECTRONIC CIRCUIT CHECKS

When the possibility of operator error has been eliminated, and the existing symptoms have been thoroughly analyzed but the cause of the problem cannot be found, then attempt to determine if the problem is repeatable, continuous, or intermittent. The identical operation should be repeated several times to determine the types and number of failures.

If repeating the operation fails to sufficiently isolate the location of the malfunctioning circuit area, all the diagnostic programs should be run to determine if the symptoms appear under all conditions.

The power supply voltages, as well as the AC line voltage at the input, should be checked first to determine if they are within specification. The basic timing circuits should then be checked. Problems in either of these areas are difficult to diagnose, since these circuits affect operation of all other circuits. These timing circuits, in turn, make error indications intermittent and problem isolation difficult. Varying the environment (power supply voltages, heat, mechanical shock, etc.) may sometimes cause an intermittent problem to occur more often so that it can be investigated more effectively.

CAUTION

The +5V should only be varied ±5% in margin tests. The IC chips used are rated from +4.75V to +5.25V.

5.4.6.1 Circuit Divisions

When attempting fault isolation in electronic systems, it is best to divide the system into troubleshooting areas, with each system unit being considered as a separate area. Then each functional section of each unit (power circuits, amplifier circuits, servo circuits, digital circuits, analog circuits, etc.) should be considered as a separate area. In this way, each area can be individually evaluated, and those not involved in the problem can be eliminated from consideration. The source of the problem is thus isolated into ever smaller areas until only the actual problem area remains.

Most electronic equipment operates from an interwoven network of circuits. Malfunctions or improper operating procedures originating in one area of the equipment often cause failure symptoms within that area and other related areas. These symptoms are the foremost troubleshooting aids available and should be used to their fullest extent. In many instances, a malfunction can be isolated to a particular area by completely analyzing the symptoms.

5.4.7 NOISE PROBLEM CHECKS

Many times, equipment failures occur which are extremely intermittent and seem to appear at random intervals. The cause of these symptoms can often be traced to the power ON/OFF switching of heavy machinery or high-powered electrical devices in the immediate area. Such events can cause extreme noise signals on the primary AC power input lines and a sudden variation in line voltage may be reflected in the DC operating voltages which can result in an equipment failure. Therefore, when extremely intermittent failures are encountered, an attempt must be made to reference these failures to a simultaneous outside occurrence which might have a bearing on the problem.

Individual power supplies within the equipment must be checked for excessive ripple in output levels. Checks must also be performed for noise bursts caused by the combination of loose electrical connections and mechanical shock or vibration. In some situations, individual components may also be found to be sensitive to mechanical shock or vibration even though all connections are secure.

5.4.8 FAULT ISOLATION GUIDE

Table 5-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the TC7000 Tape Coupler system. It lists possible symptoms, probable cause of the malfunction, and corrective actions.

Table 5-1. TC7000 Tape Coupler Fault Isolation Guide

Symptom	Probable Cause	Remedy
CPU powered up, FAULT/ACTIVITY LED indicator lit.	Self-Test failure.	Verify TC7000 Tape Coupler PCBAs are properly seated in CPU backplane; reseat if necessary. The Cable Paddleboard PCBA should be checked very carefully for proper installation. Self-Test may not pass if the Cable Paddleboard PCBA is not properly installed.
		Defective unit. Return TC7000 Tape Coupler to factory.
Data Transfer operation attempted but ACTIVITY LED not lit.	Cable for control lines or data lines reversed.	Check cable connections and reverse if pins of connectors not properly matched.
	Interface cables to/from addressed tape transport not connected.	Connect cables to/from addressed tape transport.
	Addressed tape transport does not have Ready status.	Perform operations on tape transport that are needed to produce Ready status condition.
	Wrong Base Address coded in configur-ation DIP switches.	Encode correct address in configuration DIP switch pack.
Unable to interrupt CPU.	Wrong Interrupt Vector Address coded in configuration DIP switch pack.	Encode correct Interrupt Vector Address in configuration DIP switch pack.

6.1 OVERVIEW

This section describes and defines the bit functions in the various registers, describes commands, and explains programming concepts that handle various operations in the TC7000 Tape Coupler system. Since there are more commands than there are registers, each register in the TC7000 Tape Coupler generally contributes to the performance of several functions. This section is divided into six subsections, as listed in the following table:

Subsection	Title
6.1	Overview
6.2	MBA Registers (VAX-11/750)
6.3	MBA Registers (VAX-11/780)
6.4	Device Registers
6.5	Commands
6.6	Programming Information

6.2 MBA REGISTERS (VAX-11/750)

With the VAX-11/750 CPU system, the TC7000 Tape Coupler uses six of eight MBA registers, 32 Device registers per tape transport, and 256 MBA Map registers.

NOTE

IN VAX-11/750 CPU systems, the first MBA register [MBA Configuration/Status register (MBACSR) **F28000**] and the seventh MBA register [MBA Selected Map Register (MBASMR) **F28018**] are not used, otherwise there would be eight MBA registers, plus the MBA Map registers, described in this subsection. The contents of the first MBA register are always read back as all zeros. Register MBASMR does not respond at all and a system error is generated if access to it is attempted.

The MBA registers are used to interface the TC7000 Tape Coupler with the CMI Bus in the CPU and to the tape transport(s) via the Device registers. The MBA registers and Device registers are written to (loaded) and read from under program control to initiate commands to the tape transport(s), to enable direct memory access (DMA) Write and Read (Data Transfer) operations, and to monitor status and error conditions. The contents of the MBA and Device registers are written and read as long, 32-bit words.

The MBA Map registers (Memory Addresses F28800 through F28BFC) are used to control/interpret virtual-to-physical map locations of 256 memory pages for DMA operations.

This subsection describes the format for the contents of each MBA register and explains the use and meaning of each bit. The addresses for the MBA registers are for tape transport unit zero (0) and the first MBA, and are in hexadecimal notation. Add 2000 for the second MBA, and 4000 for the third MBA. Add 80 to the Device register address for tape transport one (1), 100 for tape transport two (2), etc.

NOTE

Unless otherwise specified, bits in these register descriptions are set by logic one (1) state, and cleared or reset by logic zero (0) state.

For quick reference, Figure 6-1 shows the entire MBA register set for the VAX-11/750 configuration. The mnemonic terms for the MBA registers begin with MBA.

6.2.1 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	IBC	MMM	IE	ABT	INIT

6.2.2 MBA STATUS REGISTER (MBASR) **Base Address +08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	0	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	ERS	0	NRS	0

Figure 6-1. TC7000 Tape Coupler MBA Register Set (VAX-11/750 CPU) (SH 1 of 3)

6.2.3 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select							Byte Offset								

6.2.4 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Byte Count															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMI Byte Count															

6.2.5 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MBF		MWCK	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2.6 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				Operation			0	Physical Address							

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Address															

Figure 6-1. TC7000 Tape Coupler MBA Register Set (VAX-11/750 CPU) (SH 2 of 3)

6.2.7 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 9	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0

Physical Page Frame Number

Figure 6-1. TC7000 Tape Coupler MBA Register Set (VAX-11/750 CPU) (SH 3 of 3)

NOTE

In the descriptions of register contents in this section, no bit positions filled by a zero are described unless the zero(s) represent part of a code.

6.2.1 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	IBC	MMM	IE	ABT	INIT

This register provides five control bits for the MBA functions of the TC7000 Tape Coupler. All bits are cleared by an Initialize (INIT) command when the INIT bit in this register is set.

Ignore Byte Count (IBC) Mode - Bit 04

When this bit is set, a Write or Read operation is not terminated by the byte counter overflow. If the IE bit is also set, an Interrupt signal is generated each time the byte counter overflows. This IBC bit cannot be set while a Write or Read operation is in progress. This mode of operation is not viable with tape transports.

MBA Maintenance Mode (MMM) - Bit 03

Setting this bit places the TC7000 Tape Coupler in the Maintenance mode, which allows the diagnostic programmer to exercise and examine the contents of the registers in the TC7000 Tape Coupler. The TC7000 Tape Coupler cannot be placed in the Maintenance mode while a Data Transfer operation is in progress.

Interrupt Enable (IE) - Bit 02

When this bit is set, the TC7000 Tape Coupler can interrupt the CPU when certain conditions occur. This bit can be cleared by writing a logic zero or by issuing an INIT command (MBACR bit 00).

Abort (ABT) - Bit 01

Setting this bit initiates the Data Transfer Abort Sequence which stops any Data Transfer operation and interrupts the CPU if the IE bit (MBACR bit 02) is set.

Initialize (INIT) - Bit 00

Setting this bit clears all registers in the TC7000 Tape Coupler, including any pending commands, and aborts any Data Transfer operation in progress. This bit always returns a zero when read.

6.2.2 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	0	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	ERS	0	NRS	0

Data Transfer Busy - Bit 31

This bit is set when a Data Transfer command is received. It is cleared when the Data Transfer operation is terminated normally, or when the Data Transfer operation is aborted.

Corrected Read Data (CRD) - Bit 29

This bit is set when the data received from memory has been corrected. It is cleared by writing a logic one or by issuing an INIT command. This bit can also be cleared by subsequent receipt of a valid Data Transfer command.

Programming Error (PGE) - Bit 12

This bit is set when one or more of the following conditions exists:

a. Program attempts to initiate a Data Transfer operation while the TC7000 Tape Coupler is currently performing one.

b. Program attempts to load (Write into) registers MBAVAR, MBABCR or MBA Map registers while the TC7000 Tape Coupler is currently performing a Data Transfer operation and the IBC bit (MBACR bit 04) is reset to logic zero.

c. Program attempts to set IBC or MMM bits (MBACR bits 04 and 03, respectively) while the TC7000 Tape Coupler is performing a Data Transfer operation.

This bit is cleared by writing a logic one in this bit position, or by issuing an INIT command. This bit is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses a Device register of any formatter which the TC7000 Tape Coupler has not been configured to support. This bit is cleared by writing a logic one into this bit position or by issuing an INIT command. Setting this bit sends zero tape transport data back to the CPU and causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Massbus Control Bus Parity Error (MCPE) - BIT 17

This bit is set whenever the NED bit (MBASR bit 18) is set. It is cleared the same way NED is cleared. Setting this bit causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Attention (ATTN) - Bit 16

This bit is asserted if any of the Attention Active (ATA) bits in the Attention Summary register (TMAS), are asserted to indicate that a tape transport in the system requires attention. Asserting this bit causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Data Transfer Completed (DTC) - Bit 13

This bit is set when the commanded Data Transfer operation is terminated by normal completion or by an error condition. It is cleared by writing a logic one in this bit position or by issuing an INIT command. This bit is also cleared by subsequent receipt of

a valid Data Transfer command. Setting this bit causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when the commanded Data Transfer operation is aborted for any reason. This bit is cleared by writing a logic one into this bit position or by issuing the INIT command. This bit is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit causes an Interrupt signal to be sent to the CPU if the IE bit (MBACR bit 02) is set.

Data Late (DLT) - Bit 11

This bit is set during a Read operation if the read buffer overflows. This bit is set during a Write or Write Check operation if the write buffer underflows. This bit is cleared by writing a logic one into this bit position or by issuing an INIT command. It is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit aborts any Data Transfer operation that is in progress.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a Compare error is detected in the upper byte while the TC7000 Tape Coupler is performing a Write Check operation. It is cleared by writing a logic one into this bit position or by issuing an INIT command. It is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit aborts any Data Transfer operation that is in progress.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a Compare error is detected in the lower byte while the TC7000 Tape Coupler is performing a Write Check operation. It is cleared by writing a logic one into this bit position or by issuing an INIT command. This bit is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit aborts any Data Transfer operation that is in progress.

Missed Transfer Error (MXE) - Bit 08

This bit is set when an illegal command in the range from 2D through 3F is received. The ILF bit in device Error Register (TMER bit 00) is set at the same time this bit is set. This bit is cleared by writing a logic one into this bit position or by issuing an INIT command. This bit is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit aborts any Data Transfer operation that is in progress.

Invalid Map (IM) - Bit 04

This bit is set when the Valid bit of the next Page Frame Number is zero and the byte counter is not zero (see Map register description). This bit is cleared by writing a logic one into this

bit position or by issuing an INIT command. Setting this bit aborts any Data Transfer operation that is in progress.

Error Confirmation (ERS) - Bit 03

This bit is set when the MBA receives error confirmation for a Read or Write command. It is cleared by writing a logic one into this bit position, by issuing a Data Transfer command, or by issuing an INIT command. Setting this bit aborts any Data Transfer operation that is in progress.

No Response Status (NRS) - Bit 01

This bit is set when the TC7000 Tape Coupler receives no response from memory during a DMA operation. The set condition of this bit indicates that the effective physical memory address was nonexistent. This bit is cleared by writing a logic one into this bit position or by issuing an INIT command. This bit is also cleared by subsequent receipt of a valid Data Transfer command. Setting this bit aborts any Data Transfer operation that is in progress.

6.2.3 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select								Byte Offset							

This register contains the 17-bit Virtual Address for the commanded Data Transfer operation.

Bits <08:00> select the byte within the page and bits <16:09> select one of the 256 Map Registers. Bits <23:17> can be read from or written to, but they have no function or effect. Bits <31:24> always return logic zeros and are unused.

The 9-bit byte offset is concatenated with the 15-bit physical page address obtained from the addressed map register to form the 24-bit physical CMI Bus address. The Virtual Address is incremented by four after every memory Read or Write operation is completed and does not point to the next byte to be transferred if the Data Transfer operation does not end on a long-word boundary. Also, when a Write Check error is detected, the Virtual Address register does not point to the failing memory address because the data buffer was preloaded. The Virtual Address of the bad data may be found by determining the number of bytes actually transferred by the tape transport and adding the difference to the initial Virtual Address.

6.2.4 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Byte Count															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMI Byte Count															

This register contains the byte count for the number of bytes transferred to or from the tape transport and for the number of bytes transferred to or from the memory. The two Data Transfer operations stop when the byte counts reach zero. The program initially loads the two's complement of the number of bytes for the Data Transfer operation into bits <15:00> of this register. The TC7000 Tape coupler then loads this value into bits <31:16>.

6.2.5 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MBF		MWCK	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register cannot be written into unless the MMM bit MBACR bit 03) is set. Unless explicitly written into, this register reads a hexadecimal BF for data. This register is cleared to the BF condition whenever the INIT bit (MBACR bit 00) is set. Only bits <31:21> are Read/Write bits; all other bits are Read-only bits. Only the bits described in the following paragraphs are emulated.

Simulated Sync Clock (SSCK) - Bit 27

Setting this bit sets the Maintenance Write Clock (MWCK bit 18) in this register.

Simulated Attention (SATN) - Bit 24

Setting this bit sets the ATTN bit (MBASR bit 16) in the MBA Status Register.

Massbus Fail (MBF) - Bit 20

This bit is a reflection of the MMM bit (MBACR bit 03).

Maintenance Write Clock (MWCK) - Bit 18

The state of this bit is always a reflection of the state of the SSCK bit (MBADR bit 27) in this register.

6.2.6 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				Operation			0	Physical Address							

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Physical Address															

This contents of this Read-only register are valid only when a DMA operation is in progress or has just been completed. This register contains the byte mask, operation code, and the physical address of the last DMA operation completed by the TC7000 Tape Coupler.

6.2.7 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 9	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0
	Physical Page Frame Number														

The TC7000 Tape Coupler contains 256 Map Registers at physical base address + <800:BFC>. The Map Registers are used to form the CMI Bus physical memory address that is derived form the 17-bit Virtual Address contained in register MBAVAR. Map Registers can be written into (loaded) only when no Data Transfer operation is in progress or when the IBC bit (MBACR bit 04) is set. An attempt to Write to a Map Register during a Data Transfer operation with the IBC bit cleared (reset to logic zero), is ignored and causes the PGE bit (MBASR bit 19) to be set.

Valid Bit (V) - Bit 31

When set, indicates PFN coded in bits <PFN14:PFN00> is a valid entry.

Not Used - Bits <30:15>

Always reset to return a logic zero when read.

Physical Page Frame Number (PFN) - Bits <14:00>

These bits contain the high-order bits of the physical memory address.

6.3 MBA REGISTERS (VAX-11/780)

The TC7000 Tape Coupler contains eight MBA registers, 32 Device Registers per tape transport, and 256 MBA Map registers. The MBA registers are used to interface the TC7000 Tape Coupler with the SBI Bus in the CPU and to the tape transport(s) via the Device registers. The MBA registers and Device registers are written to (loaded) and read from under program control to initiate commands to the tape transport(s), to enable direct memory access (DMA) Write and Read (Data Transfer) operations, and to monitor status and error conditions. The contents of the MBA and Device registers are written and read as long, 32-bit words.

The MBA Map Registers (Base Address + 800 through Base Address + BFC) are used to control/interpret virtual-to-physical map locations of 256 memory pages for DMA operations.

NOTE

Base Address depends on the TR number, as listed in the following table:

20008000	-	TR4
2000A000	-	TR5
2000C000	-	TR6
2000E000	-	TR7
20010000	-	TR8
20012000	-	TR9
20014000	-	TR10
20016000	-	TR11

This subsection describes the format for the contents of each MBA register and explains the use and meaning of each bit. The addresses for the MBA registers are for tape transport unit zero (0) and the first MBA, and are in hexadecimal notation. Add 2000 for the second MBA, and 4000 for the third MBA. Add 80 to the Device register address for tape transport one (1), 100 for tape transport two (2), etc.

NOTE

Unless otherwise specified, bits in these register descriptions are set by logic one (1) state, and cleared or reset by logic zero (0) state.

For quick reference, Figure 6-2 shows the entire MBA register set for the VAX-11/780 configuration. The mnemonic terms for the MBA registers begin with MBA.

6.3.1 MBA CONFIGURATION/STATUS REGISTER (MBACSR) **Base Address**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WDS	URD	0	MT	XF	0	0	PD	PU	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

6.3.2 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MMM	IE	ABT	INIT

6.3.3 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	RDS	ITO	RTO

Figure 6-2. TC7000 Tape Coupler MBA Register Set (VAX-11/780 CPU) (SH 1 of 3)

6.3.4 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select							Byte Offset								

6.3.5 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Byte Count															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI Byte Count															

6.3.6 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN					MBF		MWCK	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3.7 MBA SELECTED MAP REGISTER (MBASMR) **Base Address + 18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	PFN 20	PFN 19	PFN 18	PFN 17	PFN 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PFN 15	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 0	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0

Figure 6-2. TC7000 Tape Coupler MBA Register Set (VAX-11/780 CPU) (SH 2 of 3)

6.3.8 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				VMI Physical Address											

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VMI Physical Address															

6.3.9 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	PFN 20	PFN 19	PFN 18	PFN 17	PFN 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PFN 15	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 9	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0

Physical Page Frame Number

Figure 6-2. TC7000 Tape Coupler MBA Register Set (VAX-11/780 CPU) (SH 3 of 3)

6.3.1 MBA CONFIGURATION/STATUS REGISTER (MBACSR) **Base Address**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PE	WDS	URD	0	MT	XF	0	0	PD	PU	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SBI Parity Error (PE) - Bit 31

This bit is set when an SBI parity error is detected. It is cleared by power failure or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Write Data Sequence (WDS) - Bit 30

This bit is set when no write data is received after a Write command has been issued. It is cleared by power failure or by

de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Unexpected Read Data (URD) - Bit 29

This bit is set when unexpected read data is received. It is cleared by power failure or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Multiple Transfer (MT) - Bit 27

This bit is set when the ID on the SBI does not agree with the transmitted ID while the TC7000 Tape Coupler is transmitting information on the SBI. It is cleared by power failure or by de-assertion of the Fault signal. Setting this bit causes the Fault signal to be asserted on the SBI.

Transmit Fault (XF) - Bit 26

This bit is set when SBI Fault signal is detected while the TC7000 Tape Coupler is transmitting information on the SBI Bus. It is cleared by power failure or by de-assertion of the Fault signal.

Coupler Power Down (PD) - Bit 23

This bit is set when the TC7000 Tape Coupler receives an asserted AC LO signal. It is cleared when power to the TC7000 Tape Coupler goes up, or by assertion of INIT, UNJAM, or DC LO signals, or by writing a one into this bit position. Setting this bit causes an Interrupt to be sent to the CPU if Interrupt Enable (IE) (MBACR bit 02) is set.

Coupler Power Up (PU) - Bit 22

This bit is set when the TC7000 Tape Coupler receives de-assertion of the AC LO signal. It is cleared when power to the TC7000 Tape Coupler goes down, or by assertion of INIT, UNJAM, or DC LO, or by writing a one into this bit position. Setting this bit sets bit IE (MBACR bit 02) and causes an Interrupt to be sent to the CPU.

Adapter Code - Bits <07:00>

Each type of Massbus Adapter (MBA) is assigned a unique code to identify it. The code for this MBA device is 00100000; therefore, a hexadecimal 20 is always read from the low order 16 bits of this register.

6.3.2 MBA CONTROL REGISTER (MBACR) **Base Address + 04**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	MMM		IE	ABT INIT

Bit descriptions for this register are the same as those in subsection 6.2.1, except bit 04 always returns a zero for a VAX-11/780 CPU.

6.3.3 MBA STATUS REGISTER (MBASR) **Base Address + 08**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DTB	NRC	CRD	0	0	0	0	0	0	0	0	0	PGE	NED	MCPE	ATTN

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	DTC	DTA	DLT	WCU	WCL	MXE	EXC	0	0	IM	EC	RDS	ITO	RTO

All bits in this register, except DTB, NED and ATTN, are cleared by writing a one into the bit position, or by setting the INIT bit (MBACR bit 00), or by subsequent receipt of a valid Data Transfer command.

Data Transfer Busy (DTB) - Bit 31

This Read-only bit is set when a Data Transfer command is received. It is cleared when the Data Transfer operation is terminated normally or when the Data Transfer operation is aborted. No Interrupt can occur if DTB is set to logic one.

No Response Confirmation (NRC) - Bit 30

This bit is set when the TC7000 Tape Coupler receives no response confirmation for the command or write data sent on the SBI. Setting this bit causes a retry of the command.

Corrected Read Data (CRD) - Bit 29

This bit is set when data received from memory has been corrected.

Programming Error (PGE) - Bit 19

This bit is set when there exists one or more of the following conditions:

a. Program tries to initiate a Data Transfer operation when the TC7000 Tape Coupler is currently performing a Data Transfer operation.

b. Program tries to load MBAVAR, MBABC, or Map registers while the TC7000 Tape Coupler is currently performing a Data Transfer operation.

c. Program tries to establish Maintenance mode while the TC7000 Tape Coupler is currently performing a Data Transfer operation.

When this bit is set, the Data Transfer operation is not aborted. If bit IE is set to logic one, then an Interrupt occurs at the end of the Data Transfer operation. Since the Interrupt is caused by completion of the Data Transfer operation, PGE set does not cause the Interrupt condition but does retain the Interrupt condition if it is not cleared and if bit IE remains set.

Nonexistent Drive (NED) - Bit 18

This bit is set when the program addresses any device register for a tape transport that does not exist. Setting this bit sends zero tape transport data back to the CPU and causes an Interrupt to the CPU if the IE bit is set.

Massbus Control Bus Parity Error (MCPE) - Bit 17

This bit is set when NED is set.

Attention (ATTN) - Bit 16

This Read-only bit is asserted if any of the Attention Active (ATA) bits in register TMAS are asserted. Asserting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Transfer Completed (DTC) - Bit 13

This bit is set whenever a Data Transfer operation is terminated because of normal completion or because of an error condition. Setting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Transfer Aborted (DTA) - Bit 12

This bit is set when a Data Transfer operation is aborted for any reason. Setting this bit causes an Interrupt to the CPU if the IE bit is set.

Data Late (DLT) - Bit 11

This bit is set during a Read operation if the data buffer overflows, or during a Write or Write Check operation if the data buffer underflows. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Upper Error (WCU) - Bit 10

This bit is set when a Compare error is detected in the upper byte while the TC7000 Tape Coupler is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Write Check Lower Error (WCL) - Bit 09

This bit is set when a Compare error is detected in the lower byte while the TC7000 Tape Coupler is performing a Write Check operation. Setting this bit aborts the Data Transfer operation that is currently in progress.

Missed Transfer Error (MXE) - Bit 08

This bit is set when there exists one or more of the following conditions:

a. An illegal command in the range from 2D to 3F is received; ILF (TMER bit 00) is set.

b. A Data Transfer operation is attempted while ERR is set, MOL is cleared, or VV is cleared (TMDS bits 14, 12, and 06, respectively).

Setting this bit aborts the Data Transfer operation that is currently in progress.

Exception (EXC) - Bit 07

This bit is set to indicate an Error condition was detected during a Data Transfer operation between the TC7000 Tape Coupler and the selected tape transport. Setting this bit aborts the Data Transfer operation that is currently in progress.

Invalid Map (IM) - Bit 04

This bit is set when the Valid (V) bit of the next page frame number is zero and the byte count is not zero. Setting this bit aborts the Data Transfer operation that is currently in progress.

Error Confirmation (EC) - Bit 03

This bit is set when the TC7000 Tape Coupler receives a bus error confirmation for a Read or Write command. Setting this bit aborts the Data Transfer operation that is currently in progress.

Read Data Substitute (RDS) - Bit 02

This bit is set when the Read Data received from memory is indicated to be Read Data Substitute. Setting this bit aborts the Data Transfer operation that is currently in progress.

Interface Sequence Timeout (ITO) - Bit 01

This bit is set when the TC7000 Tape Coupler receives a bus error confirmation, or when it fails to receive response confirmation before 102.4 microseconds have elapsed after the command was initially sent on the SBI. Setting this bit aborts the Data Transfer operation that is currently in progress.

Read Data Timeout (RTO) - Bit 00

This bit is set when the TC7000 Tape Coupler fails to receive Read Data before 102.4 microseconds have elapsed after the Read command was initially sent on the SBI. Setting this bit aborts the Data Transfer operation that is currently in progress.

6.3.4 MBA VIRTUAL ADDRESS REGISTER (MBAVAR) **Base Address + 0C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Map Select					Byte Offset										

Bit descriptions for this register are the same as those in subsection 6.2.3; except bits <23:17> are Read-only and return all zeros when read.

6.3.5 MBA BYTE COUNT REGISTER (MBABCR) **Base Address + 10**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Byte Count															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SBI Byte Count															

Bit descriptions for this register are the same as those in subsection 6.2.4.

6.3.6 MBA DIAGNOSTIC REGISTER (MBADR) **Base Address + 14**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				SSCK			SATN				MBF		MWCK		
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit descriptions for this register are the same as those in subsection 6.2.5.

6.3.7 MBA SELECTED MAP REGISTER (MBASMR) **Base Address + 18**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	PFN 20	PFN 19	PFN 18	PFN 17	PFN 16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PFN 15	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 9	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0

This register contains the contents of the last legal MBA Map register used during the last DMA operation.

6.3.8 MBA COMMAND ADDRESS REGISTER (MBACAR) **Base Address + 1C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte Mask				VMI Physical Address											
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VMI Physical Address															

The contents of this Read-only register are valid during and after a DMA operation. This register contains the byte mask on the VMI, and the VMI Physical Address of the last DMA Data Transfer operation.

6.3.9 MBA MAP REGISTERS **Base Address + <800:BFC>**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
V	0	0	0	0	0	0	0	0	0	0	PFN 20	PFN 19	PFN 18	PFN 17	PFN 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PFN 15	PFN 14	PFN 13	PFN 12	PFN 11	PFN 10	PFN 9	PFN 8	PFN 7	PFN 6	PFN 5	PFN 4	PFN 3	PFN 2	PFN 1	PFN 0

Physical Page Frame Number

Bit descriptions for this register are the same as those in subsection 6.2.7, except <PFN20:PFN00> are used for the physical page frame number instead of <PFN14:PFN00>, and only bits <30:21> return all zeros when read.

6.4 DEVICE REGISTERS

The TC7000 Tape Coupler contains 32 device registers for each of the tape transports. These registers are read from and written to as long 32-bit words. When any of the Device registers are read from, the upper 16 bits of each Device register is the same as the upper half of register MBASR in bits <31:16>. The addresses for the device registers are for formatter/tape transport unit zero, and they are shown in hexadecimal offsets from the Base Address. The last 22 Device registers are not used by the TC7000 Tape Coupler and have illegal addresses (Base Address + 440 through Base Address + 47C). Attempts to access these addresses causes the Illegal Register (ILR) error bit (TMER bit 01) to be set.

For quick reference, Figure 6-3 shows the entire Device register set for both VAX-11/750 and VAX-11/780 CPU configurations. All Device registers have mnemonic symbols beginning with TM.

6.4.1 CONTROL REGISTER 1 (TMCS1) **Base Address + 400**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DVA										F4	F3	F2	F1	F0	GO

6.4.2 DRIVE STATUS REGISTER (TMDS) **Base Address + 404**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	EOT	0	DPR	DRY	SSC	PES	SDWN	IDB	TM	BOT	SLA

6.4.3 ERROR REGISTER (TMER) **Base Address + 408**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COR/ CRC	UNS	OPI	DTE	NEF	CS/ ITM	FCE	NSG	PEF/ LRC	INC/ VPE	DPAR	FMT	CPAR	RMR	ILR	ILF

6.4.4 MAINTENANCE REGISTER (TMMR) **Base Address + 40C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TSC															

6.4.5 ATTENTION SUMMARY REGISTER (TMAS) **Base Address + 410**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

6.4.6 FRAME COUNT REGISTER (TMFC) **Base Address + 14**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 9	FC 8	FC 7	FC 6	FC 5	FC 4	FC 3	FC 2	FC 1	FC 0

Figure 6-3. TC7000 Tape Coupler Device Register Set (SH 1 of 2)

6.4.7 DRIVE TYPE REGISTER (TMDT) **Base Address + 18**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NSA	TAP	0	0	0	SPR	0	0	0	0	1	0	1	1	0	0

Formatter/Tape Transport Type

6.4.8 CHECK CHARACTER REGISTER (TMCK) **Base Address + 1C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4.9 SERIAL NUMBER REGISTER (TMSN) **Base Address + 20**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW4 8	SW4 7	SW4 6	SW4 5	SW4 4	SW4 3	SW4 2	SW4 1	FR 4	FR 3	FR 2	FR 1	FR 0	UN 2	UN 1	UN 0

Option Switches | Firmware Revision | Unit No.

6.4.10 TAPE CONTROL REGISTER (TMCR) **Base Address + 24**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACCL	FCS	SAC	EAO DTE	0	DEN 2	DEN 1	DEN 0	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	EV PAR	SS2	SS1	SS0

Figure 6-3. TC7000 Tape Coupler Device Register Set (SH 2 of 2)

6.4.1 CONTROL REGISTER 1 (TMCS1) **Base Address + 400**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DVA										F4	F3	F2	F1	F0	GO

This Write/Read register receives operational commands from the CPU. The selected tape transport responds to the 14 function codes listed in Table 6-1. If register TMCS1 is loaded with a function code (with GO bit set) that is not listed in Table 6-1, the ILF bit (TMER bit 00) is set. The function codes defined in Table 6-1 are listed and described in subsection 6.5, Table 6-2.

Table 6-1. Control Register Function Codes

Function Code Bits						Function Code Number In Hexadecimal Notation	Command
F4 05	F3 04	F2 03	F1 02	F0 01	GO 00		
0	0	0	0	0	1	01	NO OP
0	0	0	0	1	1	03	REWIND OFF LINE
0	0	0	1	1	1	07	REWIND
0	0	1	0	0	1	09	DRIVE CLEAR
0	0	1	0	1	1	11	READ-IN PRESET
0	0	1	1	1	1	15	ERASE
0	1	0	0	0	1	17	WRITE TAPE MARK
0	1	0	0	1	1	19	SPACE FORWARD
0	1	1	0	1	1	1B	SPACE REVERSE
1	0	1	0	0	1	29	WRITE CHECK FWD
1	0	1	1	1	1	2F	WRITE CHECK REV
1	1	0	0	0	1	31	WRITE FORWARD
1	1	1	0	0	1	39	READ FORWARD
1	1	1	1	1	1	3F	READ REVERSE

6.4.2 DRIVE STATUS REGISTER (TMDS) **Base Address + 404**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	EOT	0	DPR	DRY	SSC	PES	SDWN	IDB	IM	BOT	SLA

This Read-only register stores tape system status information.

Attention Active (ATA) - Bit 15

Setting this bit also sets the ATTN bit (MBASR bit 16). When set, it indicates one of the following conditions:

a. The TC7000 Tape Coupler and the selected tape transport require servicing.

b. The TC7000 Tape Coupler and the selected tape transport have become Ready after completion of an operation that did not require data to be transferred.

c. A tape transport status change has occurred.

Composite Error (ERR) - Bit 14

This bit is set whenever any bit in the Error register (TMER) is set. When set, indicates an error condition has occurred.

Positioning In Process (PIP - Bit 13

This bit is set by the TC7000 Tape Coupler during execution of a Space command or by the selected tape transport during a Rewind operation. When set, indicates the selected tape transport is performing a tape motion operation that does not transfer any data.

Medium On-Line (MOL) - Bit 12

When set, indicates the selected tape transport has tape loaded and that selected tape transport is in On-Line mode; i.e., under computer control, not under operator manual control (Off-Line mode).

Write Lock (WRL) - Bit 11

When set, indicates the selected tape transport is Write Protected.

End of Tape (EOT) - Bit 10

When set, indicates the selected tape transport has detected the EOT marker during forward tape motion. EOT signal is negated when the EOT marker is detected during reverse tape motion.

Not Used - Bit 09

Always reset to return a logic zero when read.

Drive Present (DPR) - Bit 08

This bit is a reflection of the DVA bit (TMCS1 bit 11).

Drive Ready (DRY) - Bit 07

When set, indicates the TC7000 Tape Coupler and the selected tape transport are Ready to accept a command.

Slave Status Change (SSC) Bit 06

When set, indicates the tape transport has just gone On-Line or Off-Line, or has completed a Rewind operation.

Phase Encoded Status (PES) - Bit 05

When set, indicates the selected tape transport is configured for PE operation. Reset (cleared) when selected tape transport is configured for NRZI or GCR operation.

Settle Down (SDWN) - Bit 04

When set, indicates tape motion on the selected tape transport is stopping.

Identification Burst (IDB) - Bit 03

When set, indicates a PE identification burst from the selected tape transport has been detected. Remains set (asserted) until a subsequent tape motion command is issued to that tape transport.

Tape Mark (TM) - Bit 02

When set, indicates a Tape Mark (sometimes called File Mark) has been detected on the selected tape transport. Remains set (asserted) until the next tape motion command is issued to that tape transport.

Beginning of Tape (BOT) - Bit 01

When set, indicates the selected tape transport has detected the BOT marker. Remains set until BOT marker moves beyond BOT sensor.

Slave Attention (SLA) - Bit 00

When set, indicates a selected tape transport has gone from Off-Line mode to On-Line mode.

6.4.3 ERROR REGISTER (TMER) **Base Address + 408**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COR/ CRC	UNS	OPI	DTE	NEF	CS/ ITM	FCE	NSG	PEF/ LRC	INC/ VPE	DPAR	FMT	CPAR	RMR	ILR	ILF

This Read-only register stores 16 different error conditions that can be detected and incicated in the TC7000 Tape Coupler/tape transport system.

Correctable Data Error or CRC Error (COR/CRC) - Bit 15

When set during a PE Read operation, indicates a single dead track has occurred.

When set during a NRZI Read operation, indicates the Cyclic Redundancy Check Character (CRCC) read from the tape does not match the CRCC computed from data read from the tape.

Unsafe (UNS) - Bit 14

When set, indicates one of the following conditions:

a. A program-controlled operation is being attempted on a selected tape transport that is not On Line; i.e., MOL bit (TMDS bit 12) cleared (reset to logic zero).

b. An imminent system power failure is detected (AC LO signal is present on CMI or VMI Bus).

Operation Incomplete (OPI) - Bit 13

When set during a Write, Read, or Space operation, indicates end of record has not been detected within seven seconds from beginning time of command execution. Also set during execution of Read Reverse or Space Reverse command if BOT is detected before end of specified frame count.

Drive Timing Error (DTE) - Bit 12

When set during a Write operation, indicates the selected tape transport did not receive the Write Clock (WCLK) pulse from the TC7000 Tape Coupler in time to provide a valid tape character.

Nonexecutable Function (NEF) - Bit 11

When set, indicates one of the following conditions:

a. Write operation attempted on Write Protected tape transport.

b. Space Reverse, Read Reverse, or Write Check Reverse operation attempted when tape is positioned at the BOT marker.

c. State of DEN2 bit (TMCR bit 10) in Tape Control Register does not match state of PES bit (TMDS bit 05) in Status Register during a Write operation if Enable Density Check switch SW4-8 is ON.

d. Space or Write operation attempted when FCS bit (TMCR bit 10) is reset to logic zero.

e. NRZI Write operation attempted when DEN2 bit (TMCR bit 10) is reset to logic zero, and Frame Count Register (TMFC) contains the two's complement of a number that is less than 13 (decimal).

Correctable Skew or Illegal Tape Mark (CS/ITM) - Bit 10

When set during a PE Read operation, indicates excessive but correctable skew is detected. This error indication is only an alerting notice and does not indicate bad data.

When set during a NRZI Read operation, indicates tape characters that are not legally a Tape Mark have been read and recognized as a Tape Mark.

Frame Count Error (FCE) - Bit 09

When set, indicates one of the following conditions:

a. Space operation has terminated, but frame counter is not cleared; i.e., Frame Count Register (TMFC) contains a non-zero value.

b. Data Transfer operation is completed and contents of MBA Byte Count Register (MBABCR) has not reached zero; therefore, expected data byte count stored in MBABCR is greater than actual number of bytes read or written.

Nonstandard Gap (NSG) - Bit 08

This bit can be set only during Write operation, never during Read operation. When set, indicates a tape character has been detected during the first half of the End-of-Record Gap.

Format Error or LRC Error (PEF/LRC) - Bit 07

When set during a PE Read operation, indicates an incorrect preamble or postamble has been detected.

When set during a NRZI Write operation, indicates the Longitudinal Redundancy Check Character (LRCC) read from the tape does not match the LRCC computed from the tape characters that have been read from the tape.

Incorrectable Data Error or Vertical Parity Error (INC/VPE) - Bit 06

When set during a PE Read operation, indicates detected occurrence of one of the following conditions:

a. Multiple dead tracks

b. Dead tracks without parity errors

c. Parity errors without dead tracks

d. Skew buffer overflow.

When set during a NRZI Read operation, indicates a Vertical Parity Error has occurred, or data has appeared after termination of a Skew Delay function.

Data Bus Parity Error (DPAR) - Bit 05

When set, indicates incorrect parity has been detected on the data bus link between the TC7000 and the selected tape transport.

Format (FMT) - Bit 04

When set during a Data Transfer operation, indicates use of an incorrect format code is being attempted.

Control Bus Parity Error (CPAR) - Bit 03

When set, indicates a parity error has occurred on the control bus link between the TC7000 Tape Coupler and the selected tape transport.

Register Modification Refuse (RMR) - Bit 02

When set during a tape transport operation while the GO bit (TMCS1 bit 00) is set to logic one, indicates an attempt was made to Write into one of the Device registers other than the Maintenance Register (TMMR) and the Attention Summary Register (TMAS).

Illegal Register (ILR) - Bit 01

When set, indicates an attempt was made to Write or read from a nonexistent register.

Illegal Function (ILF) - Bit 00

When set, indicates an illegal function code has been transmitted (set into the Function Code bits <TMCS1 05:00> of the Control Register).

6.4.4 MAINTENANCE REGISTER (TMMR) **Base Address + 40C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	TSC	0	0	0	0	0	0

This Read/Write register contains the system oscillator Tape Speed Clock (TSC) signal generated by the TC7000 Tape Coupler. The Frequency of this clock pulse is fixed to correspond with 125 ips (6.25 kHz) which is the same as the Clock pulse frequency used in the TU77 tape transport. This clock pulse bit is used to monitor and time tape transport operations. All bits except bit 06 in this register are Read/Write; bit 06 is Read-only.

6.4.5 ATTENTION SUMMARY REGISTER (TMAS) **Base Address + 410**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

This Write/Read register uses up to eight bit positions <07:00> to store the status of the Attention Active (ATA) signal level generated by the tape transports in the system. Each tape transport uses one particular bit position in the lowest eight bits of this register to reflect the state of its ATA bit; i.e., whether the tape transport does or does not need attention. High level or logic one indicates bit is set and tape transport needs attention. Low level or logic zero indicates bit is clear and tape transport does not need attention. ATA bit position 00 correlates to tape transport 0, ATA bit position 01 correlates to tape transport 1, and so on through ATA bit position 07:tape transport 7. Bits <15:08> of this TMAS Register are not used and return all zeros.

The TMAS register is selected by addressing any tape transport. When the contents of the TMAS register are Read, the status of the ATA bit for each tape transport in the system is immediately determined. The CPU can then selectively examine the contents of the registers for each tape transport, which has set its ATA bit, to determine the cause of the individual attention conditions.

Writing a logic one into the bit position resets the ATA bit for the tape transport assigned to that bit position, but writing a logic zero does not affect the status of that bit position. This writing method allows the CPU to reset, after inspection, all ATA bits that were set without accidentally resetting any bits that may have become set in the meantime. The results of writing into an ATA bit position in the TMAS Register are shown in the following table:

ATA Bit Before	Attention Summary Bit Written	ATA Bit After	Change
0	0	0	No
1	0	1	No
0	1	0	No
1	1	0	Yes

6.4.6 FRAME COUNT REGISTER (TMFC) **Base Address + 414**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 9	FC 8	FC 7	FC 6	FC 5	FC 4	FC 3	FC 2	FC 1	FC 0

This Write/Read register counts tape events.

For a Write operation, it contains the two's complement of the number of tape characters to be written. It is loaded before the Write command is initiated. During the Write operation, it is incremented by one each time a character is sent to the tape formatter. Normal Write Data Transfer termination is accomplished when the contents of this TMFC Register overflows to zero.

For a Space operation, it contains the two's complement of the number of records to be spaced, and it is incremented by one when the end of a record is detected. Normal termination of a Space operation is accomplished when the contents of this TMFC Register overflows to zero.

For a Read operation, the bits in this register are reset to all zeros before the Read command is initiated. This register is then incremented each time a character is received from the tape formatter. At the end of the Read operation, this register contains the two's complement of the number of characters read from the tape.

Contents of the TMFC Register may be read at any time, but can be written into only when the tape transport is not performing a Space or Data Transfer operation; i.e., GO bit (TMCS1 bit 00) reset to zero.

6.4.7 DRIVE TYPE REGISTER (TMDT) **Base Address + 418**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NSA	TAP	0	0	0	SPR	0	0	0	0	1	0	1	1	0	0
							Formatter/Tape Transport Type								

The contents of this Read-only register identify the particular type and configuration of formatter and tape transport emulation being used in the system. When the contents of this register are read, bits <DT08:DT00> contain 28 (hexadecimal) if a slave unit other than unit number zero is selected, or if unit number zero is selected but it is not on line. If the selected tape transport does exist and is on line, bits <DT08:DT00> in this register contain 2C (hexadecimal). The contents of this register always indicate a tape speed of 125 ips even though actual tape speed may be any standard tape speed.

Not Sector Addressed (NSA) - Bit 15

Always set to indicate tape transport is not sector addressable.

Tape Drive (TAP - Bit 14

Always set to indicate the device is a tape transport.

Slave Present (SPR) - Bit 10

When set, indicates selected tape transport is on line.

Drive Type (DT) - Bits <DT08:DT00>

Specifies type of formatter and tape transport (TM03 and TU77 = 2C hexadecimal). Bits DT02 through DT00 are always reset to logic zero if SPR bit (TMDT bit 10) is reset to logic zero.

6.4.8 CHECK CHARACTER REGISTER (TMCK) **Base Address + 41C**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This Read-only register is not supported in the TC7000 Tape Coupler firmware, and returns all zeros when its contents are read.

6.4.9 SERIAL NUMBER REGISTER (TMSN) **Base Address + 420**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW4 8	SW4 7	SW4 6	SW4 5	SW4 4	SW4 3	SW4 2	SW4 1	FR 4	FR 3	FR 2	FR 1	FR 0	UN 2	UN 1	UN 0
Option Switches								Firmware Revision					Unit No.		

This Read-only register contains one bits provided by settings of DIP switch SW4, a binary representation of the firmware revision level where revision A = 1, B = 2, etc., and a binary coded number that represents the unit number of the selected tape transport. (For SW4 settings, see Appendix A, Table A-2.)

6.4.10 TAPE CONTROL REGISTER (TMCR) **Base Address + 424**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACCL	FCS	SAC	EAO DTE	0	DEN 2	DEN 1	DEN 0	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	EV PAR	SS2	SS1	SS0

The contents of this 16-bit Write/Read register are used to select an existing tape transport and to configure that tape transport to a particular operational mode.

Accelleration (ACCL) - Bit 15

This Read-only bit is set when the tape transport is not actively writing or reading data.

Frame Count Status (FCS) - Bit 14

This Read-only bit is normally set at the end of writing the frame count into the Frame Count Register (TMFC). If this bit is reset to logic zero, while the GO bit (TMCS1 bit 00) is set to logic one,

and an attempt is made to execute a Space or Write command, a Nonexecutable Function (NEF) error is generated (TMER bit 11 set) and the command is not executed. This bit is reset when register TMFC overflows to zero.

Slave Address Change (SAC) - Bit 13

This Read-only bit is set whenever the Slave Select bits (TMCR bits <02:00>) are non-zero.

Enable Abort On Data Transfer Errors (EAODTE) - Bit 12

When set, this bit causes immediate abort of any in-progress Write or Read operation if a formatter-to-tape coupler Data Bus Parity error is detected.

Not Used - Bit 11

Always reset to return a logic zero when read.

Density Select (DEN2-DEN0) - Bits <10:08>

The states of these bits define tape character density during Write operations. Read-density select is done automatically and no bits in this register change state. For dual-density (or tri-density) tape transports, densities are coded as listed and defined in the following table:

DEN2	DEN1	DEN0	Density in cpi
0	X	X	800 NRZI* (bits 1 and 0 are don't care)
1	0	0	1600 PE
1	0	1	Reserved
1	1	0	Reserved
1	1	1	6250 GCR**

* For PE/GCR units, selecting NRZI density selects GCR density instead.
** Tri-density tape transports only. Requires special software to implement. Illegal unless option switches are set to make legal. See Appendices A and B.

Bits DEN2-DEN0 have no effect on single-density tape transport systems. For dual-density systems, the NRZI density selection selects one density and the PE density selection selects the other density. For the DEN2-DEN0 bits to have any effect at all in any situation, the tape transport must be configured for software density (or speed) select.

Format Select (FMT SEL3 - FMT SEL0) - Bits <07:04>

The states of these bits define the tape coupler-to-tape format during a Write operation, or the tape-to-tape coupler format during

a Read operation. Format Select codes supported by the TC7000 Tape Coupler are listed and defined in the following table:

FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	Format
1	1	0	0	PDP-11 Normal
1	1	1	0	PDP-15 Normal

PDP-15 Normal is similar to IBM format where the upper byte in each 16-bit word is the least significant byte (LSB) and the lower byte is the most significant byte (MSB). All other formats are illegal and generate a Format (FMT) error (TMER bit 04) if used.

Even Parity (EV PAR) - Bit 03

Ignored during PE and GCR operations because these operations always use odd parity.

When set during NRZI Read or Write operations, even parity is used.

Slave Select (SS2-SS0) - Bits <02:00>

The states of these bits specify the selected slave unit of the selected TM03 formatter. The TC7000 Tape Coupler supports slave unit zero only.

6.5 COMMANDS

Commands are selected by the Function Code bits in register TMCS1. Function Codes for commands are listed in Table 6-1. Commands established by the Function Codes are listed and described in Table 6-2. All commands clear the GO bit (TMCS1 bit 00) after they have been executed. All commands clear the ATA bit at the start of the operation if the ERR bit (TMDS bit 14) is reset to logic zero.

Table 6-2. Control Register Function Code Command Descriptions

Hex No.	Operation	Command Description
01	No Op	Performs no operation. Clears ATA bit in register TMDS.
03	Rewind Off-Line (Requires manual intervention to return tape transport to On-Line mode.)	Performs the following three functions: 1. Initiates Rewind operation on selected tape transport and places it in Off-Line mode. 2. Sets the following bits in Status Register (TMDS bits 15, 07, and 06, respectively): Attention Active (ATA) Drive Ready (DRY) Slave Status Change (SSC)

Table 6-2. Control Register Function Code
Command Descriptions (continued)

Hex No.	Operation	Command Description
07	Rewind	Performs the following three functions: 1. Initiates Rewind command to rewind tape on selected tape transport to Beginning of Tape (BOT) marker. 2. After initiating the Rewind operation, sets the following bits in Status Register (TMDS bits 15, 13, and 07, respectively): Attention Active (ATA) Positioning in Progress (PIP) Drive Ready (DRY) The set DRY bit causes the GO bit to be cleared as soon as the Rewind operation is started. 3. When BOT is sensed, sets bit 06 (SSC) and clears bit 13 (PIP) in Status Register (TMDS). If ATA is not still set, these TMDS conditions set ATA again and generate a second interrupt if bit IE is set to logic 1.
09	Drive Clear	In selected tape transport, performs the following functions: 1. Clears registers TMER and TMMR. 2. In register TMCR, clears FCS bit and sets ACCL bit. 3. In register TMDS, clears bits ATA and ERR. 4. If slave zero is selected, also clears bits SSC and SLA in register TMDS. 5. Drive Clear is only Op Code that can be executed if ERR bit (TMDS bit 14) is set to logic 1. Does not affect unselected tape transports in system.
11	Read-In Preset	Clears bits <13:00> in register TMCR, then causes slave 0 tape transport to Rewind to BOT.
15	Erase	Erases approximately 3 inches (7.6 cm) of tape in selected tape transport. When done, sets ATA bit (TMDS bit 15).

Table 6-2. Control Register Function Code
Command Descriptions (continued)

Hex No.	Operation	Command Description
17	Write Tape Mark	Writes special tape record on selected tape transport. When done, sets ATA bit (TMDS bit 15).
19	Space Forward	Moves tape on selected tape transport forward toward end of tape (EOT) marker over the number of tape records specified by the contents of the Frame Count Register (TMFC). Operation is aborted if Tape Mark (TM) signal or EOT signal is detected before end of specified frame count. When done (operation terminated by normal completion of command execution or by command abort), sets ATA bit (TMDS bit 15).
1B	Space Reverse	Moves tape on selected tape transport in reverse direction toward BOT marker over the number of tape records specified by the contents of register TMFC. Operation is aborted if TM or BOT signal is detected before end of specified frame count. When done, sets ATA bit (TMDS bit 15).
29	Write Check Forward	Same as Read Forward operation, except the data read from the tape is compared with the data in memory and if there is a Compare error, bit 09 or 10 in register MBASR is set.
2F	Write Check Reverse	Same as Read Reverse operation, except the data read from the tape is compared with the data in memory and if there is a Compare error, bit 09 or 10 in register MBASR is set.
31	Write Forward	Writes forward one tape record on selected tape transport. Tape record length (number of data blocks) is determined by contents of register TMFC.
39	Read Forward	Reads forward one tape record on selected tape transport. When done, the number of characters read is recorded in register TMFC.

Table 6-2. Control Register Function Code
Command Descriptions (continued)

Hex No.	Operation	Command Description
3F	Read Reverse	Reads in reverse direction one tape record from selected tape transport. When done, the number of characters read is recorded in register TMFC.

6.6 PROGRAMMING INFORMATION

This subsection explains clearing of the TC7000 Tape Coupler, interrupt conditions, termination of Data Transfer operations, and equivalent Ready-bit conditions.

6.6.1 CLEARING

The TC7000 Tape Coupler can be cleared by using any of the following methods:

a. Controller Clear -- Controller Clear is performed by writing a logic one into the INIT bit position (MBACR bit 00) or by issuing a UBUS DCLO signal. Either action causes the following register conditions for all tape transports:

- Bits <31:16> in register MBADR cleared to all zeros.
- Bits <15:00> in register MBADR set to hexadecimal BF condition.
- All bits in registers MBACR and MBASR cleared to all zeros.
- ATA bits in register TMAS cleared to all zeros, and all bits in registers TMER and TMMR cleared to all zeros.
- Bits ATA, ERR, PIP, SSC, IDB, TM and SLA in register TMDS cleared to zero.
- Bit FCS cleared and bit ACCL set in register TMCR.

b. Error Clear -- Error bits in register MBASR are cleared by writing a logic one into the bit position and by the start of another Data Transfer operation.

c. Drive Clear -- Drive Clear is a command (Function Code 09 in Tables 6-1 and 6-2). Execution of this command sets bit ACCL in register TMCR, and causes the following Device registers or bits to be cleared:

- TMMR (except bit 03) and TMER; ATA bit in TMAS; ATA and ERR bits in TMDS; FCS bit in TMCR.
- If slave zero selected in register TMCR, then bits SSC and SLA in register TMDS are also cleared.

6.6.2 INTERRUPT CONDITIONS

The TC7000 Tape Coupler generates a CPU interrupt if the Interrupt Enable (IE) bit (MBACR bit 02) is set and there exists any one of the following conditions:

a. Data Transfer operation is terminated by normal or abnormal means.

b. An Attention Active (ATA) bit has been asserted (set to logic one) in any tape transport Device register.

c. Programming Error (PGE), Nonexistent Drive (NED), or Missed Transfer Error (MXE) bit (MBASR bits 19, 18, or 09, respectively) is asserted.

d. A Power-Up (PU) or Power Down (PD) condition occurs in VAX-11/780 system; i.e., ACLO signal level changes state. Bit PU (MBACSR bit 22) set causes bit IE (MBACR bit 02) to be set and forces an Interrupt to the CPU.

The Interrupt condition persists until the register bits which caused the Interrupt are cleared.

6.6.3 DATA TRANSFER TERMINATIONS

A Data Transfer operation which has been successfully started may terminate in one of the following ways:

a. Normal Termination -- Byte counter overflows to zero and TC7000 Tape Coupler becomes Ready at end of current data block.

b. Controller Error -- Set condition is asserted at one or more of the following MBASR bit positions:

		Bit
No Response Confirmation (VAX-11/780 only)	(NRC)	30
Data Transfer Abort	(DTA)	12
Data Late	(DLT)	11
Write Check Upper Error	(WCU)	10
Write Check Lower Error	(WCL)	09
Missed Transfer	(MXE)	08
Exception	(EXC)	07
Invalid Map	(IM)	04
Error Status (VAX-11/750 only)	(ERS)	03
No Response Status (VAX-11/750 only)	(NRS)	01
Error Confirmation (VAX-11/780 only)	(EC)	03
Read Data Substitute (VAX-11/780 only)	(RDS)	02
Interface Sequence Timeout (VAX-11/780 only)	(ITO)	01
Read Data Timeout (VAX-11/780 only)	(RTO)	00

c. Drive Error -- Error (ERR) bit in register TMDS is set, and at least one bit in register TMER is set. The ATA bit for the tape transport attempting to perform the Data Transfer operation is also asserted.

d. Program-Caused Abort -- The program can terminate a Data Transfer operation by setting the Abort (ABT) or Initialize (INIT) bit (MBACR bits 01 or 00, respectively).

6.6.4 READY BITS

The Data Transfer Busy (DTB) bit (MBASR bit 31) is set when a Data Transfer operation is being executed by the TC7000 Tape Coupler. DTB is cleared when the Data Transfer operation is terminated. For Read operations, DTB is cleared when the last character has been transferred from the tape transport to the memory. For a Write operation, DTB is cleared when the last character has been sent to the tape transport. When DTB is cleared, the Data Transfer Complete (DTC) bit (MBASR bit 13) is set.

The set condition of the Drive Ready (DRY) bit (TMDS bit 07) is the Ready indicator for the selected tape transport and it is the complement of the GO bit (TMCS1 bit 00). To successfully initiate any Data Transfer command, DRY must be set and DTB must be cleared. Commands that do not involve Data Transfer operations, require setting of DRY only. Successful initiation of any command clears the DRY bit. Successful initiation of a Data Transfer command also clears bit DTC (MBASR bit 13)and sets bit DTB (MBASR bit 31). DRY (TMDS bit 07) is set when GO (TMCS1 bit 00) is reset.

BLANK

Section 7
FUNCTIONAL DESCRIPTION

7.1 OVERVIEW

This section describes the architectural organization of the TC7000 Tape Coupler and the tape formats for the tape transports supported by the TC7000 Tape Coupler. This section is divided into three subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	Architectural Organization
7.3	Tape Formats

7.2 ARCHITECTURAL ORGANIZATION

Figure 7-1 is a block diagram of the major functional elements in the TC7000 Tape Coupler VAX-11/750 organization, and Figure 7-2 is a block diagram of the major functional elements in the TC7000 Tape Coupler V-MASTER/VAX-11/780 organization. Figures 7-3 and 7-4 show the TC7000 Tape Coupler and Cable Paddleboard PCBA, respectively. The TC7000 Tape Coupler is organized around a 16-bit, high-speed bipolar microprocessor. The arithmetic logic unit (ALU) and register file portion of the microprocessor are implemented with four AMD 2901 bit-slice integrated circuit (IC) components. The microinstructions are 48 bits long, and the control memory of 4K words is implemented with six 4K x 8-bits Programmable Read-Only Memory (PROM) ICs.

The TC7000 Tape Coupler uses a 1K x 16-bits high-speed Random Access Memory (RAM) buffer to store the contents of the Massbus Adapter (MBA) Registers, Device Registers, Map Registers, and up to 512 bytes of data.

Parallel data from the selected tape transport is transferred to the RAM buffer via the microprocessor. Parallel data accessed from the RAM buffer is sent to the selected tape transport via the microprocessor. Data transfer timing is controlled by the Write Strobe and Read Strobe clock pulses.

In the VAX-11/750 CPU system, the CMI Bus is 32 bits wide. It transfers addresses and programmed I/O and DMA data. The

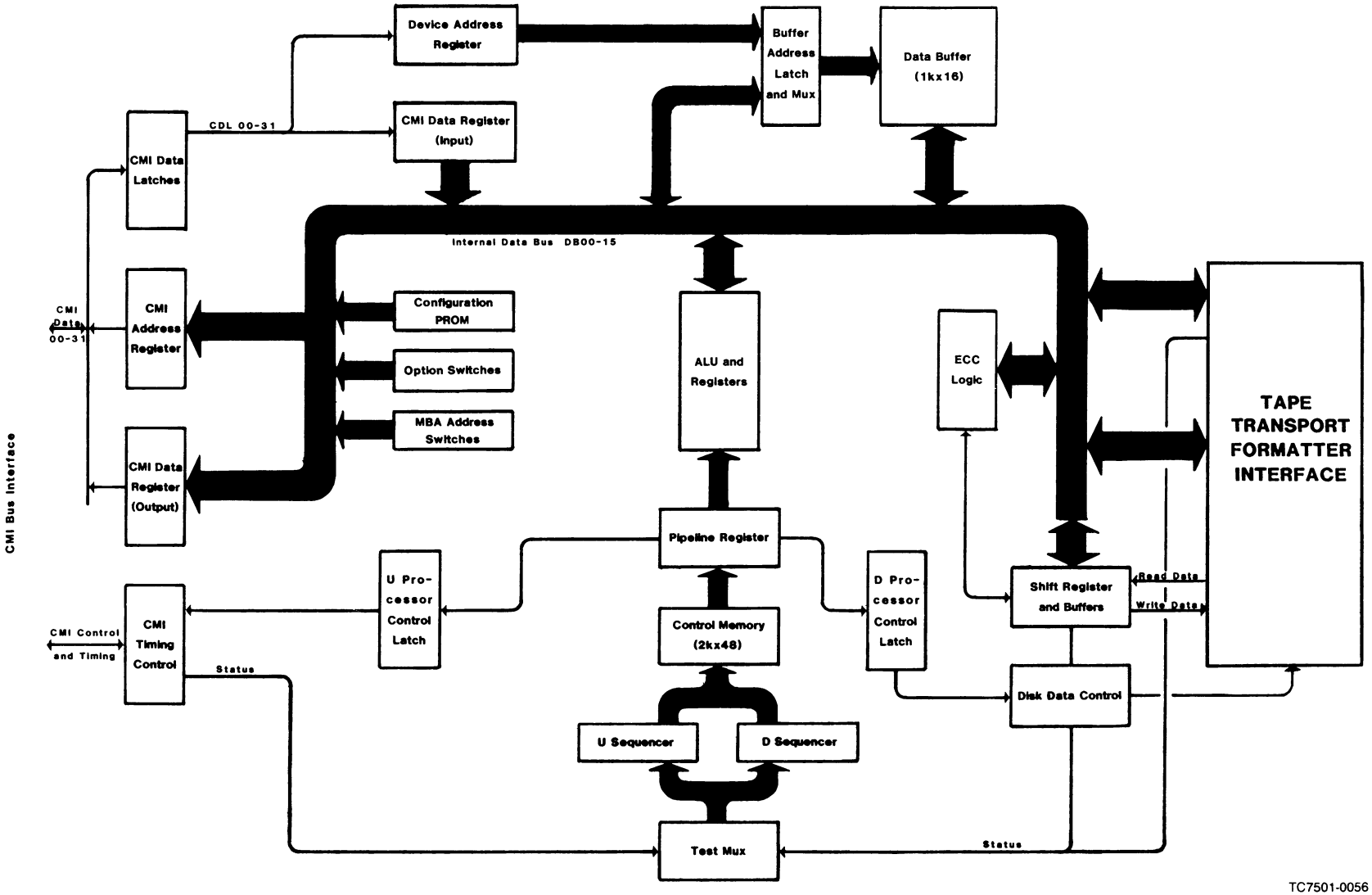


Figure 7-1. TC7000 Tape Coupler with VAX-11/750 Organization, Simplified Block Diagram

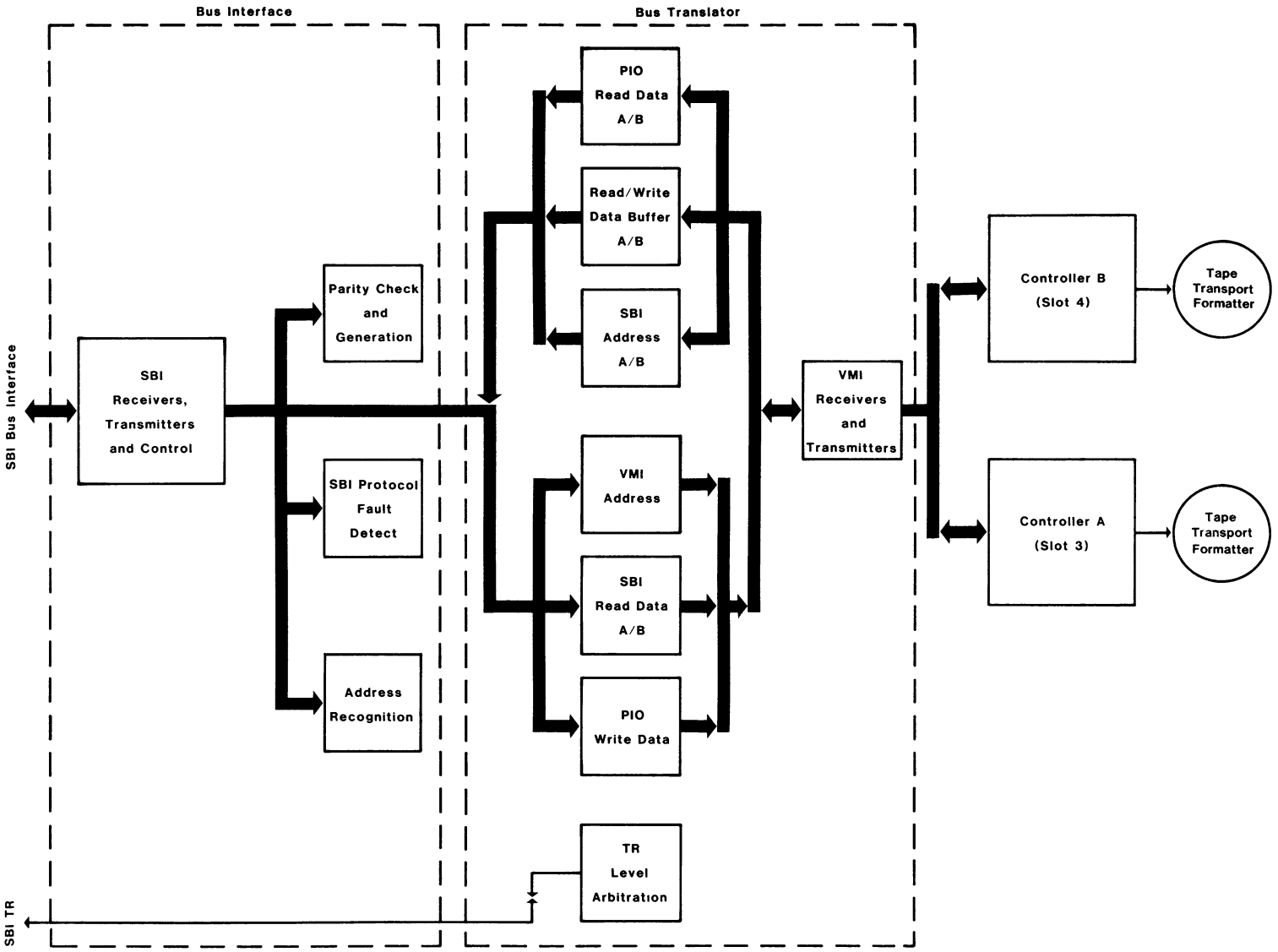


Figure 7-2. TC7000 Tape Coupler with V-MASTER/VAX-11/780 Organization, Simplified Block Diagram

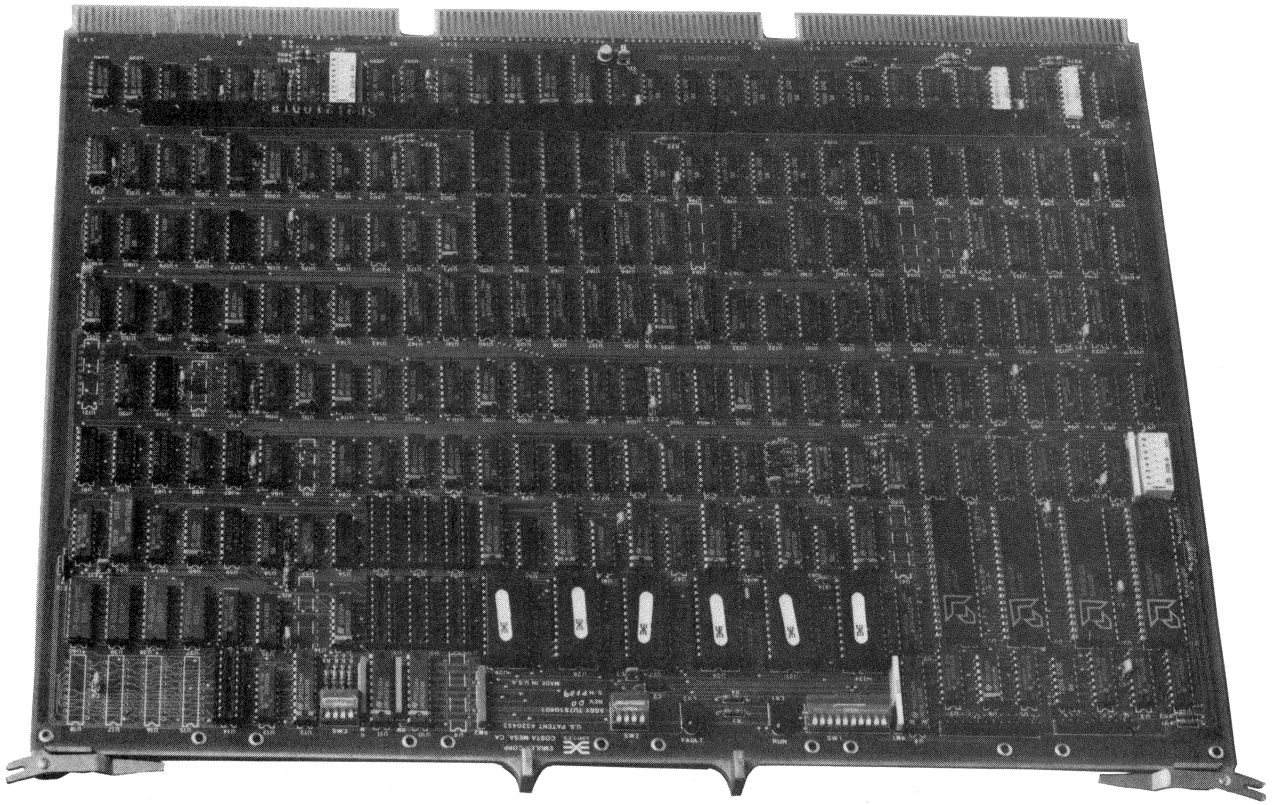


Figure 7-3. TC7000 Tape Coupler PCBA

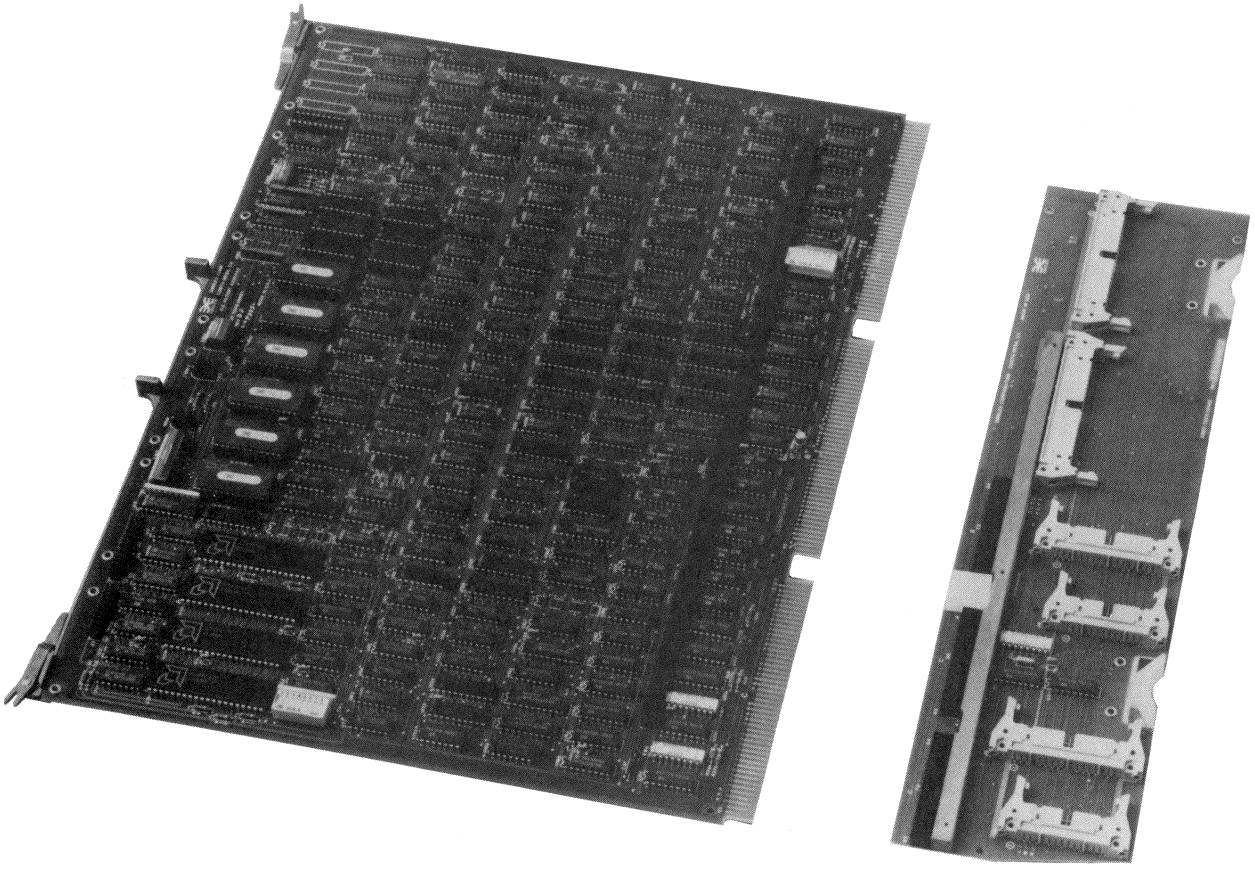


Figure 7-4. Cable Paddleboard PCBA for TC7000 Tape Coupler

microprocessor responds to all programmed I/O and does functions required for the addressed Device register. The microprocessor controls all DMA operations and transfers between the CMI Bus and the internal RAM buffer.

In the V-MASTER VAX-11/780 CPU system, the VMI Bus is 32 bits wide and is used for programmed I/O and Data Transfer operations. It transfers addresses and data. DMA operations transfer 32-bit dualwords to the V-MASTER/780, which does 64-bit quadword transfers to the SBI bus. The microprocessor responds to all programmed I/O and does functions required for the addressed Device register. The microprocessor controls all DMA operations and transfers between the VMI Bus and the internal RAM buffer.

7.2.1 V-MASTER/780

The V-MASTER/780 requires two additional PCBAs to complete the subsystem. If the TC7000 Tape Coupler is intended for use in a VAX-11/750 CPU system, these PCBAs are not required.

7.2.1.1 Bus Interface

The Bus Interface PCBA (Emulex P/N SU7810401) provides the conventional interface with the SBI of the VAX-11/780 CPU. It includes circuitry for six functions:

a. Bus transceivers

b. Parity generation and checking

c. Address tag and identification (ID) decoding

d. Sequence status logic

e. Interface and Read Data timeouts

f. SBI fault detection.

7.2.1.2 Bus Translator

The Bus Translator PCBA (Emulex P/N SU7810409) provides signal translation between the SBI output from the Bus Interface PCBA and the TC7000 Tape Coupler PCBA (Emulex P/N TU7510401). The TC7000 Tape Coupler PCBA interfaces with the Bus Translator PCBA via the V-MASTER Interface (VMI) Bus. The VMI Bus permits two Emulex Tape Couplers or Disk Controllers to be used as part of the V-MASTER. The Bus Translator PCBA provides the SBI arbitration logic, storage for programmed I/O address and data, and storage of direct memory access (DMA) addresses and data. Its primary function is to buffer between the quadword DMA on the SBI and the dualword transfer to the VMI. When doing Write operations, memory data words are automatically prefetched and transferred to the buffers on the Bus Translator PCBA to enable more efficient operation of the VMI Bus. The Bus Translator PCBA provides DMA buffering capability for two

TC7000 Tape Couplers, or a combination of a TC7000 Tape Coupler and an Emulex VAX-compatible disk controller. The TC7000 Tape Coupler requires a Bus Translator PCBA of Revision Level E or later.

7.2.2 CABLE PADDLEBOARD PCBA

The Cable Paddleboard PCBA is used to connect the TC7000 Tape Coupler to the system tape transports. It is plugged directly onto the backside (male connector) of the CPU or V-MASTER backplane slot occupied by the TC7000 Tape Coupler; therefore it interfaces with the TC7000 Tape Coupler and the CMI/VMI bus via the TM03/TU77 emulation in the TC7000 Tape Coupler PCBA. The Cable Paddleboard PCBA contains six connectors (and associated gating circuits). Two of those connectors, J1 and J2, provide cable connections to interface Pertec tape transports with the TC7000 Tape Coupler. The other four connectors, J3 through J6, provide cable connections to interface STC tape transports with the TC7000 Tape Coupler. The J3/J4 cable connectors interface with the A4 connector on the STC formatter. The J5/J6 cable connectors interface with the B4 connector on the STC formatter. If both STC and Pertec cables are connected simultaneously, errors **always** result.

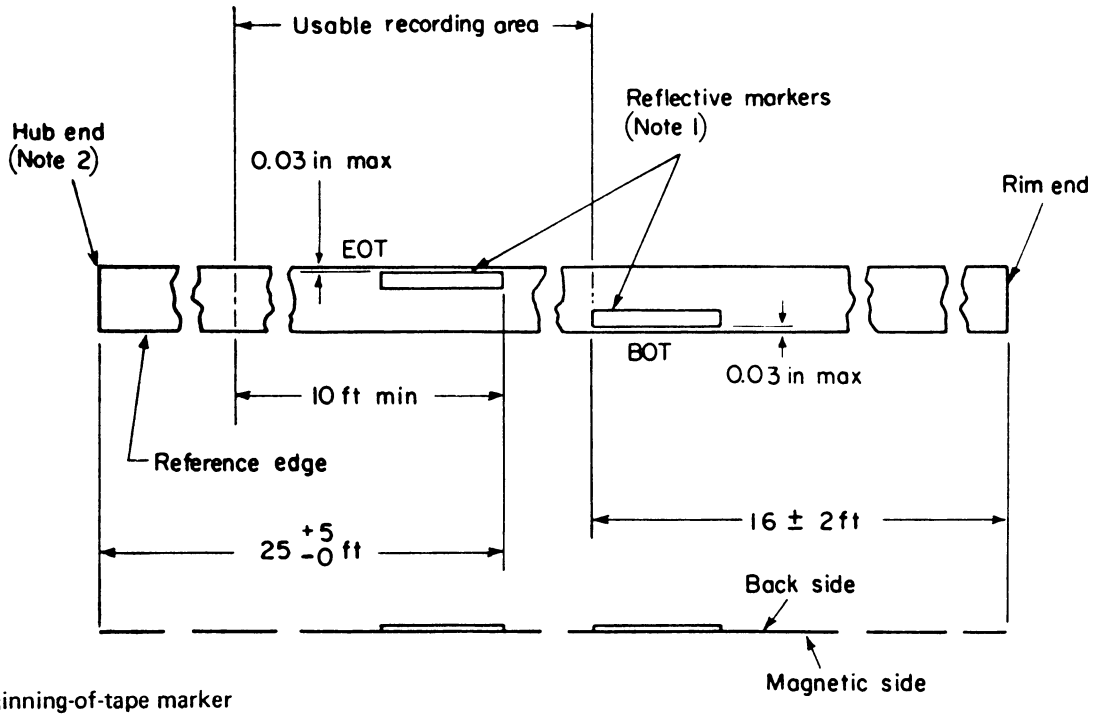
7.3 TAPE FORMATS

The TC7000 Tape Coupler can be used with tape transports that use NRZI, PE, or GCR formats. Since the TC7000 Tape Coupler interfaces only with the formatter that controls the tape transport, and never "sees" the tape transports directly, it is not concerned with tape speed or format. Any combination of format and tape speed that results in a Data Transfer rate of up to 1.5 megabytes/second can be accommodated. The three most commonly used 9-track formats are described in the following paragraphs.

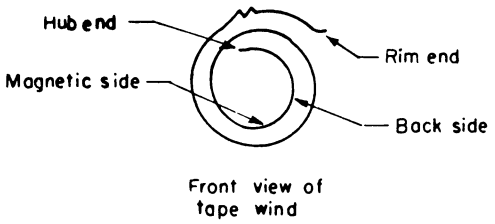
7.3.1 NRZI FORMAT

The NRZI format is the 800 cpi NRZI format specified in the American National Standards Institute (ANSI) Standard X3.22-1973.

The usable recording area of the NRZI format is shown in Figure 7-5, and the NRZI recording format is shown in Figure 7-6.



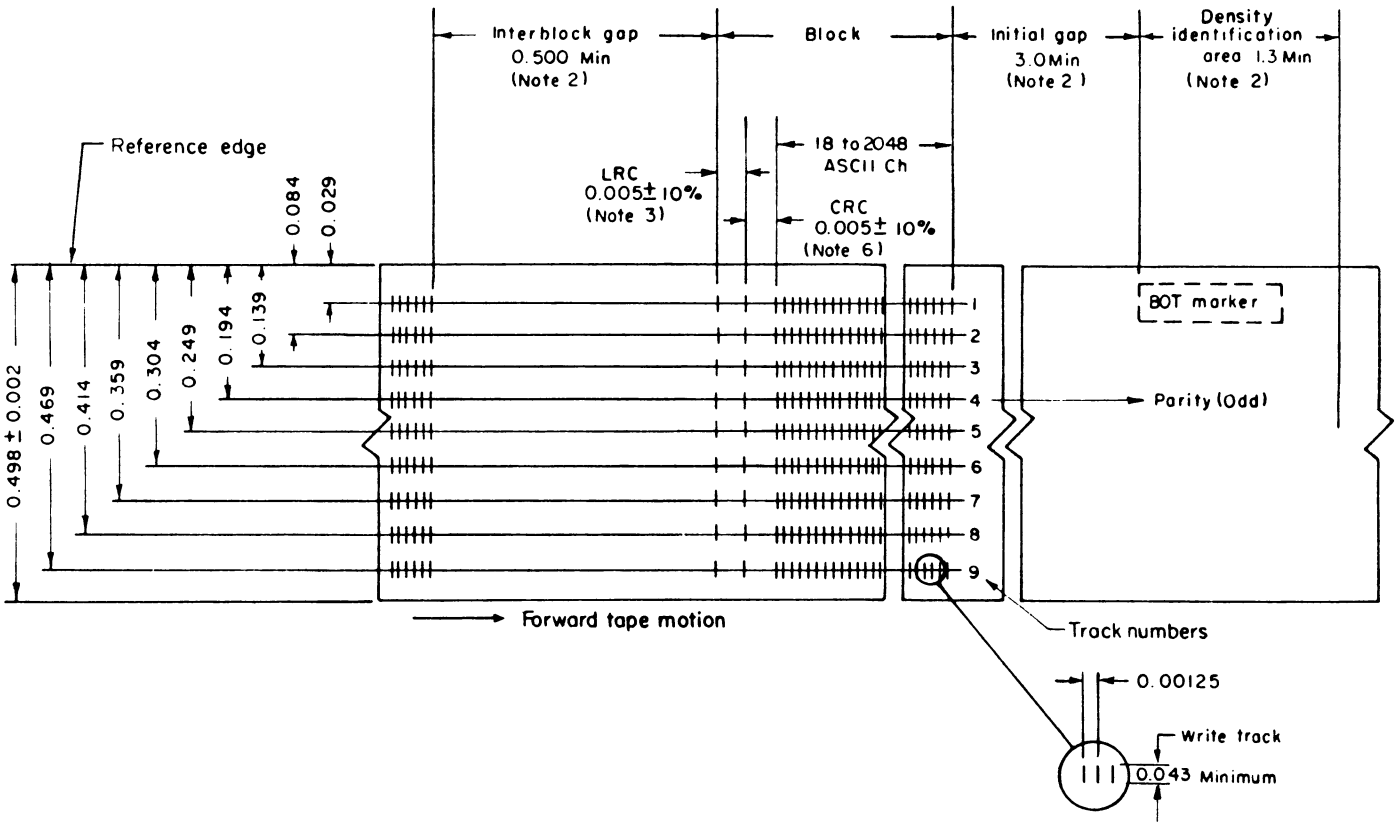
BOT: Beginning-of-tape marker
EOT: End-of-tape marker



NOTES:
(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.
(2) Tape shall not be attached to the hub.

TC7501-0258

Figure 7-5. Usable Recording Area in 800 cpi NRZI Format



Legend

BOT: Beginning of tape
Ch: Characters
CPI: Characters per inch
CRC: Cyclic redundancy check
LRC: Longitudinal redundancy check
Min: Minimum

NOTES:

(1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
(2) Tape to be fully saturated in the erased direction in the interblock gap, the initial gap, and density identification area.
(3) A longitudinal redundancy check bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the longitudinal redundancy check character.
(4) All dimensions are given in inches.
(5) There is a track placement tolerance of ± 0.003 inch for each track.
(6) Parity of CRC character is odd, if an even number of data characters are written.

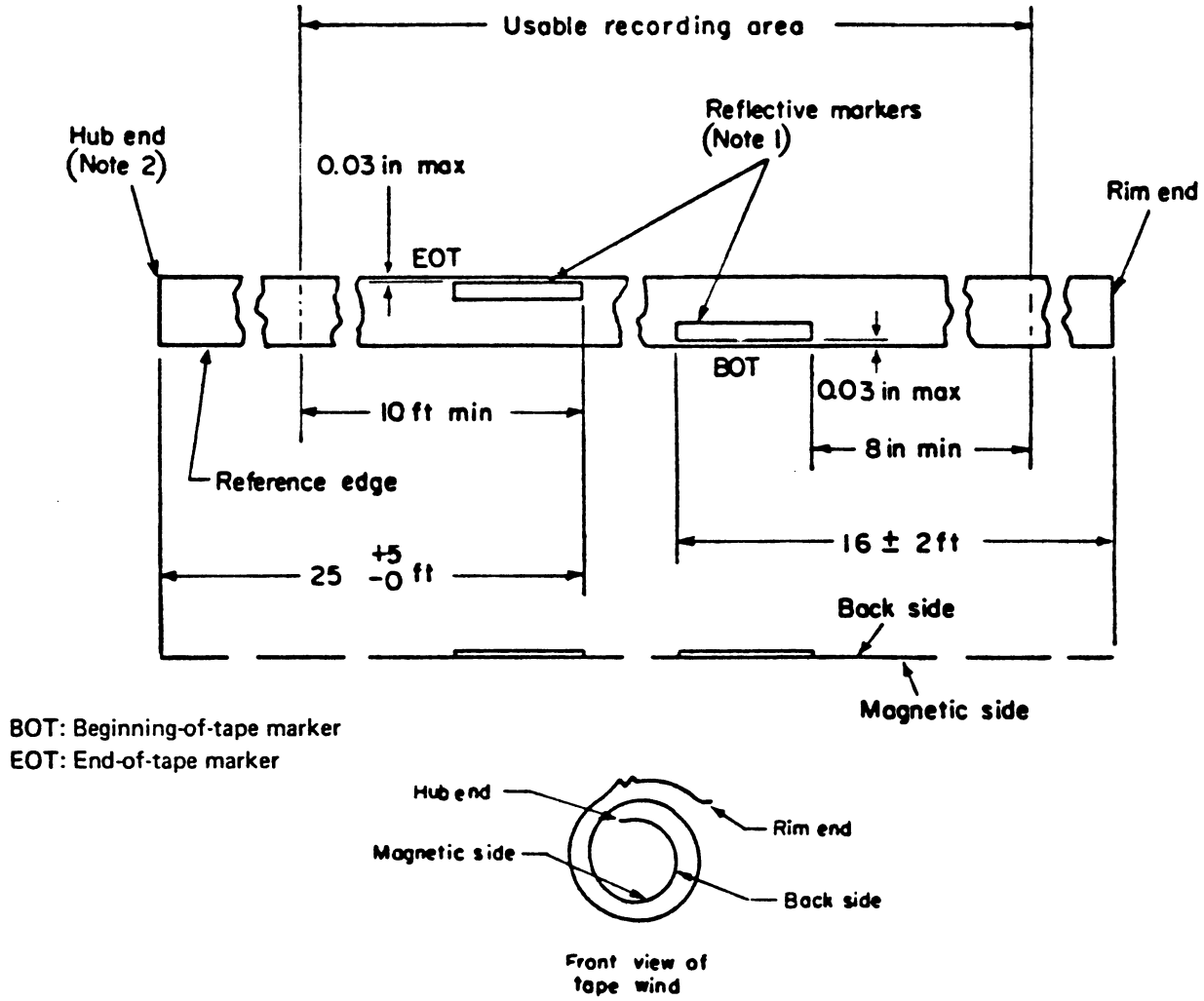
TC7501-0259

Figure 7-6. NRZI Recording Format

7.3.2 PE FORMAT

The PE format is the 1600 cpi PE format specified in the ANSI Standard X3.39-1973.

The usable recording area of the PE format is shown in Figure 7-7, and the PE recording format is shown in Figure 7-8.



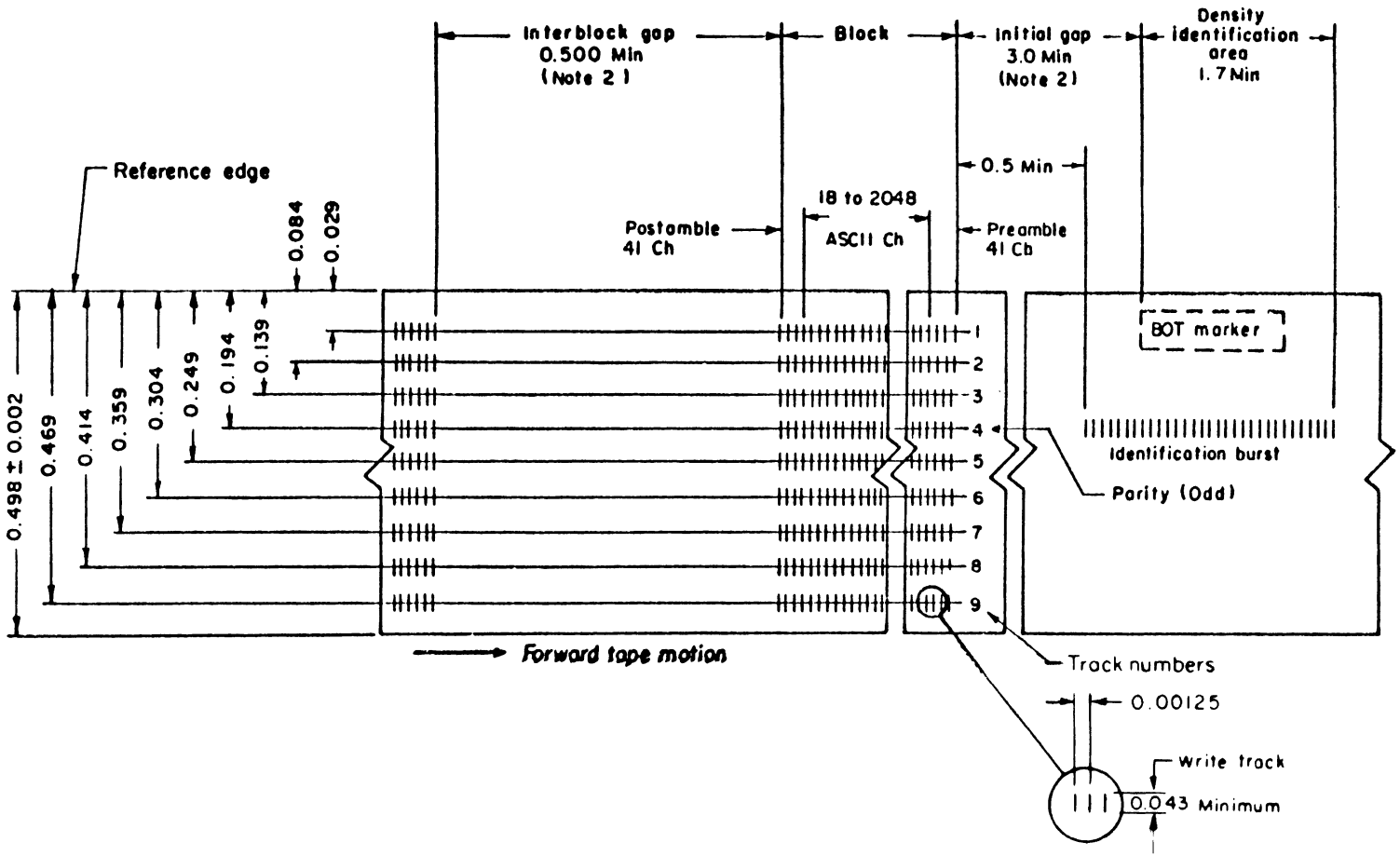
NOTES:

(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

TC7501-0260

Figure 7-7. Usable Recording Area in 1600 cpi PE Format



Legend

BOT: Beginning of tape
Ch: Characters
CPI: Characters per inch
Min: Minimum

NOTES:

(1) Tape is shown with oxide side up, Read/Write head on same side as oxide.
(2) Tape to be fully saturated in the erased direction in the interblock gap and the initial gap.
(3) The identification burst extends past the trailing edge of the BOT marker.
(4) All dimensions are given in inches.
(5) There is a track placement tolerance of ± 0.003 inch for each track.

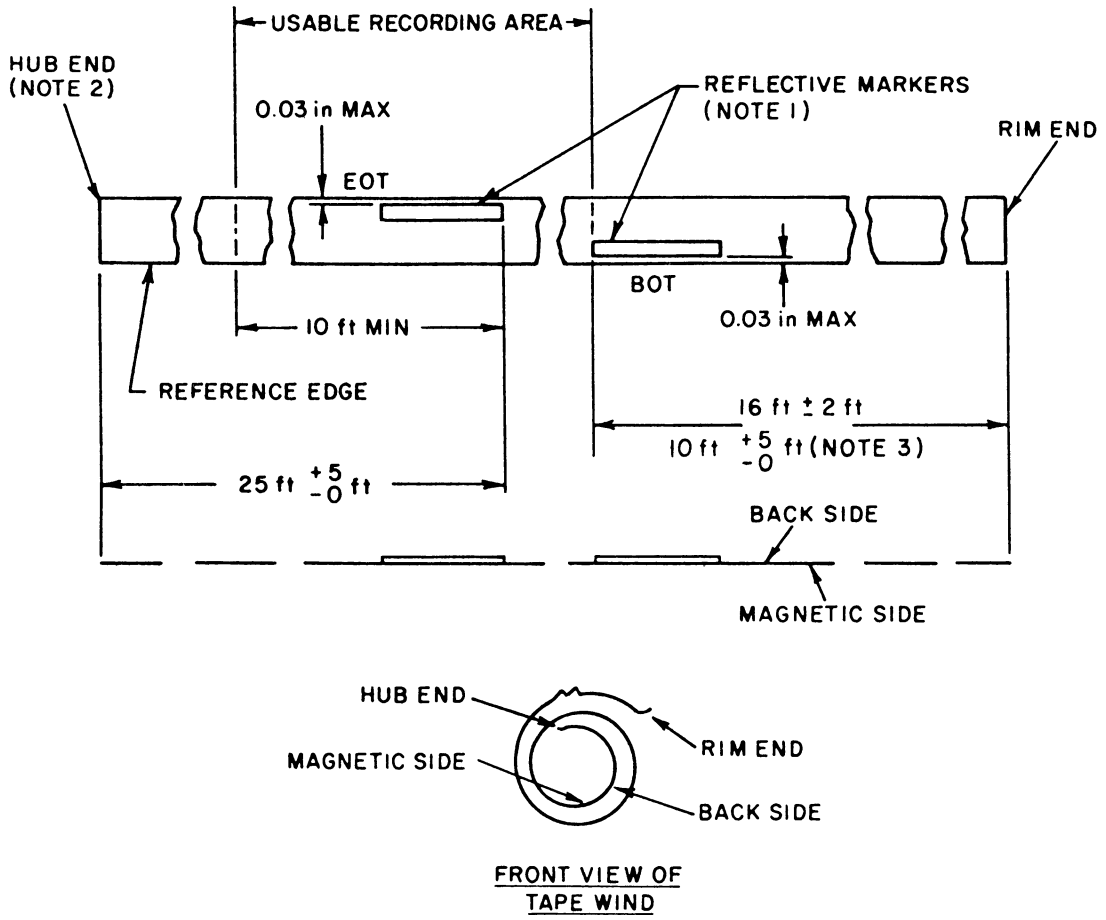
TC7501-0261

Figure 7-8. PE Recording Format

7.3.3 GCR FORMAT

The GCR format is the 6250 cpi GCR format specified in the ANSI Standard X3.54-1976.

The usable recording area of the GCR format is shown in Figure 7-9, the GCR recording format is shown in Figure 7-10, and the group organization of the GCR format is shown in Figure 7-11.



Legend

BOT: Beginning-of-tape marker

EOT: End-of-tape marker

NOTES:

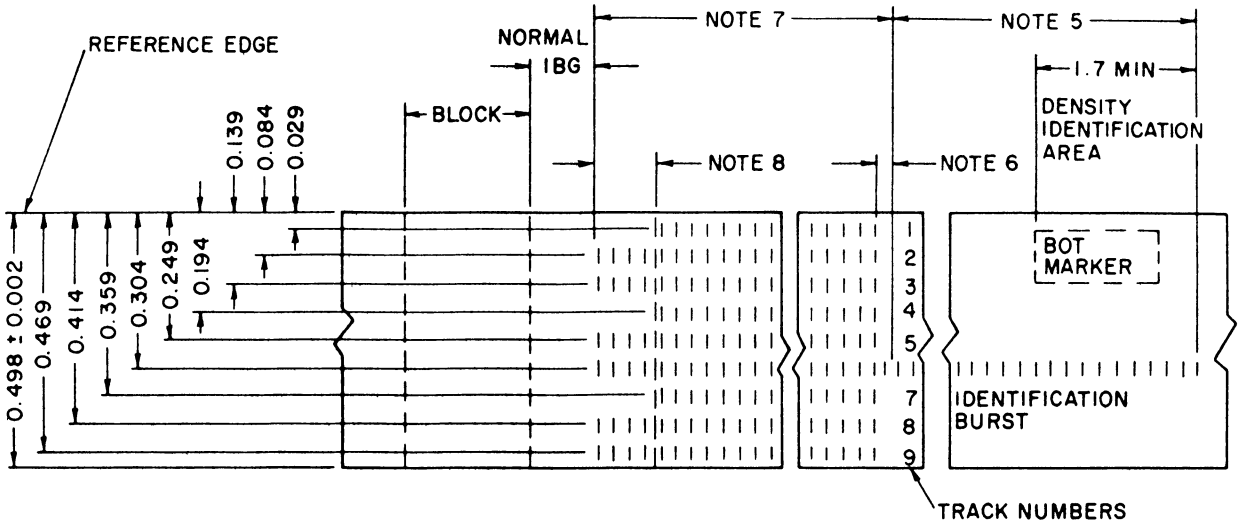
(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

(3) Two values for placement of the BOT marker are given, both of which can be handled by most tape units. The indicated value of 16 feet ± 2 feet is the current specified dimension.

TC7501-0262

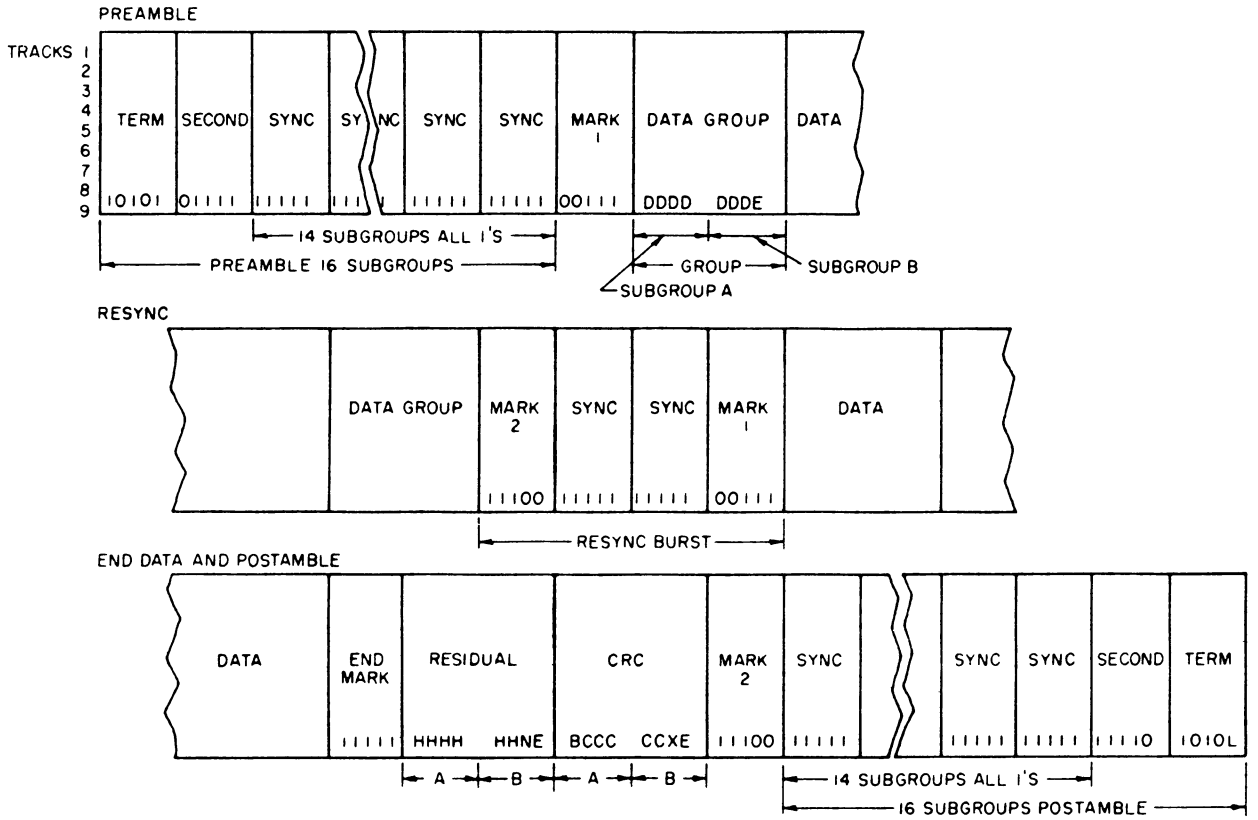
Figure 7-9. Usable Recording Area in 6250 cpi GCR Format



NOTES:
(1) Tape is shown in 6250 mode, oxide side up.
(2) All dimensions are given in inches.
(3) Track placement tolerance is ± 0.003 for each track.
(4) Tape to be fully saturated in the erase direction in the interblock gap and the ID area.
(5) ID burst (see 5.8).
(6) Undefined gap (see 5.9).
(7) ARA burst (see 5.9).
(8) ARA ID characters (see 5.9).

TC7501-0263

Figure 7-10. GCR Recording Format



Legend:

D: Data characters	C: CRC character
H: Pad or data character	N: Auxiliary CRC character
X: Residual character	L: Last character
E: ECC character	B: CRC or pad character

NOTE: This figure portrays the format prior to the encoding of the data, residual, and CRC groups in accordance with Table 2. The control subgroups are recorded on tape as shown and described.

TC7501-0264

Figure 7-11. Group Organization of GCR Recording Format

Figure 7-11. Group Organization of GCR Recording Format

8.1 OVERVIEW

The TC7000 Tape Coupler has a direct plug-in interface with the CMI Bus on the VAX-11/750 CPU backplane, or with the VMI Bus via the V-MASTER/780 backplane for the SBI when used in VAX-11/780 CPU systems. It also has Cable Paddleboard PCBA connectors for cable interface with Pertec or STC tape transport(s).

This section lists pin/signal assignments for the CPU, V-MASTER and tape transport interfaces, and is divided into six subsections as listed in the following table:

Subsection	Title
8.1	Overview
8.2	Tape Transport Interfaces
8.3	Tape Coupler CMI/VMI Interface
8.4	V-MASTER/780 SBI Pin/Signals
8.5	Bus Interface PCBA Pin/Signals
8.6	Bus Translator PCBA Pin/Signals

8.2 TAPE TRANSPORT INTERFACES

The TC7000 Tape Coupler is designed to interface with Pertec or STC tape transports, but not both types at the same time. System tape transports must be all Pertec or all STC models.

NOTE

In the L/H column in the tables of this subsection, the asserted (active) state of signal L = Low and H = High.

8.2.1 PERTEC TAPE TRANSPORT INTERFACE

Interface for Pertec tape transports is provided by connectors J1 and J2 on the Cable Paddleboard PCBA. Table 8-1 lists and describes pin assignments for all signals at this interface.

Table 8-1. TC7000 Tape Coupler and Pertec Tape Transport Interface

J1 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
2	IFBY	FBSY	L	C72
4	ILWD	LWD	L	C27
6	IW04	WD03	L	B81
8	IGO	GO	L	B67
10	IW00	WD07	L	B76
12	IW01	WD06	L	B78
14	SPARE	TEST POINT A	-	---
16	SPARE	TEST POINT B	-	---
18	IREV	REV	L	B64
20	IREW	REW	L	B60
22	IWP	WDP	L	C05
24	IW07	WD00	L	B75
26	IW03	WD04	L	B79
28	IW06	WD01	L	B80
30	IW02	WD05	L	B77
32	IW05	WD02	L	B82
34	IWRT	WRT	L	B63
36	ITHR02	RTH02	L	B61
38	IEDIT	EDIT	L	B69
40	IERASE	ERASE	L	B68
42	IWFM	WFM	L	B70
44	ITHR01	TEST POINT C	-	---
46	ITAD00	TAD00	L	C07
48	IR02	RD05	L	C76
50	IR03	RD04	L	C79

J2 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
1	IRP	RDP	L	C84
2	IROO	RD07	L	C78
3	IR01	RD06	L	C80
4	ILDP	ST01	L	C69
6	IR04	RD03	L	C75
8	IR07	RD00	L	C83
10	IR06	RD01	L	C82
12	IHER	ST06/ST06 LATCH	L	C11, C56
14	IFMK	ST02/ST02 LATCH	L	C16, C66
16	ICCG/IDENT	ST03/ST03 LATCH	L	C14, C67
18	IFEN	FEN	L	B57
20	IR05	RD02	L	C77
22	IEOT	ST10/ST10 LATCH	L	C15, C57
24	IOFL	OFL	L	B59
26	INRZ	ST05	L	C71
28	IRDY	ST07	L	C55
30	IRWD	ST13	L	C64

Table 8-1. TC7000 Tape Coupler and Pertec Tape Transport Interface (continued)

J2 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
32	IFPT	ST11	L	C58
34	IRSTR	RSTR/XRSTR	L	B84, C86
36	IWSTR	WSTR	L	C88
38	IDBY	ST14	L	C68
40	ISPD	TEST POINT D	-	---
42	ICER	ST15/ST15 LATCH	L	C18, C62
44	IONL	ST08	L	C61
46	ITAD01	TAD01	L	C10
48	IFAD	FAD	L	C08
50	IDEN/IHISP	DEN	L	B66
All odd-numbered pins are GND unless otherwise specified.				

8.2.2 STC TAPE TRANSPORT INTERFACE

Interface for STC tape transports is provided by connectors J3, J4, J5, and J6 on the Cable Paddleboard PCBA. Table 8-2 lists and defines pin assignments for all signals at this interface.

Table 8-2. TC7000 Tape Coupler and STC Tape Transport Interface

J3 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
1	AD00	TA01	L	C10
3	AD01	TA00	L	C07
5	CMD00	CMD00	L	B68
7	CMD01	CMD01	L	B69
9	CMD02	CMD02	L	B70
11	CMD03	CMD03	L	B63
13	DS00	DS00	L	B65
15	START	START	L	B67
17	STOP	STOP/STOP D	L	B64, B86
19	TRAK	TRAK	L	B83
21	DATA-P	SWDP	L	C06, C84
23	DATA-00	SWD07	L	C23, C78
25	DATA-01	SWD06	L	C26, C80
27	DATA-02	SWD05	L	C27, C76
29	DATA-03	SWD04	L	C22, C79
31	DATA-04	SWD03	L	C19, C75
33	DATA-05	SWD02	L	C20, C77
All even-numbered pins <J3-2:J3-34> are GND unless otherwise specified.				

Table 8-2. TC7000 Tape Coupler and STC Tape Transport Interface (continued)

J4 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
2	REWS	ST13	L	C64
4	FPTS	ST11	L	C58
6	BOTS	ST01	L	C69
8	EOTS	ST10	L	C57
10	OSC	N/C	-	---
12	SSC	ST14	L	C68
14	SLX02	SLX02	L	B61
16	DS01	DS01	L	B66
18	SLX00	SLX00	L	B59
20	SLX01	SLX01	L	B60
22	RESET	RESET	L	B57
24	DATA-07	SWD00	L	C24, C83
26	DATA-06	SWD01	L	C25, C82
All odd-numbered pins <J4-1:J4-25> are GND unless otherwise specified.				
J5 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
1	ERRMX-P	ERMXP	H	C34
3	ERRMX-0	ERMX00	H	C40
5	ERRMX-1	ERMX01	H	C39
7	ERRMX-2	ERMX02	H	C38
9	ERRMX-3	ERMX03	H	C37
11	ERRMX-4	ERMX04	H	C32
13	ERRMX-5	ERMX05	H	C31
15	ERRMX-6	ERMX06	H	C36
17	ERRMX-7	ERMX07	H	C35
19	BUSY	FBSY	L	C72
21	TREQ	WSTR	L	C88
23	RECV	TEST POINT K	-	---
25	IDBURST	ST03	L	C67
27	OP INC	ST12	L	C65
29	ENDATP	ENDST	L	C81
31	TMS	ST02	L	C66
33	REJECT	ST09	L	C59
All even-numbered pins <J5-2:J5-34> are GND unless otherwise specified.				

Table 8-2. TC7000 Tape Coupler and STC Tape Transport Interface (continued)

J6 Pin	Signal at Tape Transport	Signal at CPU Backplane	L/H	TC7000 Tape Coupler Connector Pin(s)
2	RESERVED	TEST POINT L	-	---
4	RESERVED	TEST POINT M	-	---
6	WRTS	TEST POINT N	-	---
8	RDYS	ST07	L	C55
10	HDENS	ST04	L	C70
12	ONLS	ST08	L	C61
14	BUPER	BUSPE	H	C33
16	NRZI	ST05	L	C71
18	BLOCK	BLOCK/BLKLTH	L	C17, C63
20	CRERR	ST15	L	C62
22	ROMPS	ROMPS	H	C29
24	DATA CHK	ST06	L	C56
26	OVRNS	POVRN/OVRNS	L/H	B85, C30
All odd-numbered pins <J6-1:J6-25> are GND unless otherwise specified.				

NOTE

The Cable Paddleboard PCBA contains five additional signal lines that terminate in jumper connections or test points as listed in the following table:

TC7000 Tape Coupler Connector Pin	Signal	L/H	Test Point
B58	DRV14	L	G
B56	DRV13	L	F
B55	DRV12	L	E
C60	ST00	L	J
B62	DRV11	L	H

8.3 TAPE COUPLER CMI/VMI INTERFACE

The tri-state CMI/VMI Interface is 32 bits wide. It transfers addresses and data in a multiplexed manner. The CPU accesses the RAM buffer and registers in the TC7000 Tape Coupler by means of this interface for Write and Read operations, and the TC7000 Tape Coupler uses this bus for DMA Data Transfer operations to and from memory.

The entire VMI/CMI interface is provided by three female connectors in the backplane into which the three PCBA edge connectors, A, B,

and C, are inserted. All three connectors have the same number of pins, but pin/signal assignments differ on each connector.

Table 8-3 lists and describes pin assignments for all signals at this interface.

NOTE

In Table 8-3, the L/H column defines the asserted (active) state of the signal. H = High and L = Low. Pins without signals defined are not used. Jumpers are described in Appendix B. Side 1 is component side of PCBA, and side 2 is solder side of PCBA.

8.3.1 ARBITRATION LEVEL

The arbitration level establishes the priority of the TC7000 Tape Coupler for obtaining access to the CMI/VMI Bus. Levels three, two, or one may be selected by setting appropriate DIP switches on the TC7000 Tape Coupler (see Section 4). These three levels are below the Unibus Interface, which is level four.

8.3.2 BR (INTERRUPT) PRIORITY LEVEL

The TC7000 Tape Coupler is hardwired at the factory for BR5 Interrupt. The other Bus Grant signals are jumpered through.

8.3.3 REGISTER ADDRESS

The Base Address for MBA registers and Device registers are specified in Section 6.

8.3.4 INTERRUPT VECTOR ADDRESS

In the VAX-11/750 CPU system, the three Interrupt Vector Addresses that correlate to the Base Addresses are: 150, 154, and 158. Selection of the Base Address for the TC7000 Tape Coupler automatically selects the appropriate Interrupt Vector Address (see Section 6 and Appendix A).

8.3.5 DCLO SIGNAL

The TC7000 Tape Coupler is held in a Reset condition as long as the Unibus DC Low (UBUS DCLO) signal is asserted. When the asserted UBUS DCLO signal is cleared, the TC7000 Tape Coupler executes its built-in Self-Test routine. The Unibus Initialize (UBUS INIT) signal is not used by the TC7000 Tape Coupler.

Table 8-3. Pin/Signal Assignments, TC7000 Tape Coupler PCBA

Side 1 Signal	Connector A L/H	Connector A Pin	Connector A Pin	Connector A L/H	Side 2 Signal
NOT USED		1	2		NOT USED
NOT USED		3	4		NOT USED
NOT USED		5	6		NOT USED
NOT USED		7	8		NOT USED
PRESENT	L	9	10		NOT USED
NOT USED		11	12		NOT USED
NOT USED		13	14		NOT USED
NOT USED		15	16		NOT USED
NOT USED		17	18		NOT USED
NOT USED		19	20		+5V
NOT USED		21	22		NOT USED
0V		23	24		0V
NOT USED		25	26		NOT USED
NOT USED		27	28		NOT USED
NOT USED		29	30		NOT USED
NOT USED		31	32		NOT USED
NOT USED		33	34		NOT USED
NOT USED		35	36		NOT USED
NOT USED		37	38		+5V
NOT USED		39	40		NOT USED
DMA EN	H	41	42	H	CLR
NOT USED		43	44		NOT USED
NOT USED		45	46		NOT USED
NOT USED		47	48	L	780 ST
DMA READ	H	49	50	L	DMA SEI
NOT USED		51	52		NOT USED
NOT USED		53	54		NOT USED
NOT USED		55	56	L	MBA SEL 0
NOT USED		57	58		+5V
NOT USED		59	60		NOT USED
NOT USED		61	62		NOT USED
NOT USED		63	64		NOT USED
NOT USED		65	66		NOT USED
BG4 IN	H	67	68	H	BG4 OUT
BG5 IN	H	69	70	H	BG5 OUT
0V		71	72		0V
BG6 IN	H	73	74	H	BG6 OUT
NOT USED		75	76		NOT USED
BG7 IN	H	77	78	H	BG7 OUT
NOT USED		79	80	L	BUS BR5
NOT USED		81	82		NOT USED
NOT USED		83	84	L	CMI ARB 1
CMI ARB 2	L	85	86	L	CMI ARB 3
CMI ARB 4	L	87	88	L	CMI ARB 5
CMI ARB 6	L	89	90	L	CMI ARB 7
-15V		91	92	L	CMI HOLD
CMI WAIT	L	93	94		NOT USED

Table 8-3. Pin/Signal Assignments, TC7000
Tape Coupler PCBA (continued)

Side 1 Signal	Connector B L/H	Connector B Pin	Connector B Pin	Connector B L/H	Side 2 Signal
CMI DATA 00	H	1	2		NOT USED
CMI DATA 01	H	3	4	H	CMI DATA 02
CMI DATA 03	H	5	6	H	CMI DATA 04
CMI DATA 05	H	7	8	H	CMI DATA 06
CMI DATA 07	H	9	10	H	CMI DATA 08
NOT USED		11	12	H	CMI DATA 09
CMI DATA 10	H	13	14	H	CMI DATA 11
CMI DATA 12	H	15	16	H	CMI DATA 13
CMI DATA 14	H	17	16	H	CMI DATA 15
CMI DATA 16	H	19	20		+5V
CMI DATA 17	H	21	22	H	CMI DATA 18
0V		23	24		NOT USED
CMI DATA 19	H	25	26	H	CMI DATA 20
CMI DATA 21	H	27	28	H	CMI DATA 22
NOT USED		29	30	H	CMI DATA 23
CMI DATA 24	H	31	32	H	CMI DATA 25
CMI DATA 26	H	33	34	H	CMI DATA 27
CMI DATA 28	H	35	36	H	CMI DATA 29
CMI DATA 30	H	37	38		+5V
CMI DATA 31	H	39	40	L	CMI STATUS 00
CMI STATUS 01	L	41	42	L	CMI DBBZ
NOT USED		43	44		0V
CMI BCLK	L	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50		NOT USED
0V		51	52		0V
0V		53	54		NOT USED
DRV12	L	55	56	L	DRV13
FEN/RESET	L	57	58	L	DRV14
OFL/SCX00	L	59	60	L	REW/SLX01
RTH02/SCX02	L	61	62	L	DRV11
WRT/CMD03	L	63	64	L	REV/STOP
LGAP/DS00	L	65	66	L	DEN/DS01
GO/START	L	67	68	L	ERASE/CMD00
EDIT/CMD01	L	69	70	L	WFM/CMD02
NOT USED		71	72		NOT USED
NOT USED		73	74	H	RUN
WD00	L	75	76	L	WD07
WD05	L	77	78	L	WD06
WD04	L	79	80	L	WD01
WD03	L	81	82	L	WD02
TRAK	L	83	84	L	XRSTR
POVRN	L	85	86	L	STOPD
+5V		87	88		NOT USED
NOT USED		89	90		NOT USED
NOT USED		91	92		0V
NOT USED		93	94		NOT USED

Table 8-3. Pin/Signal Assignments, TC7000
Tape Coupler PCBA (continued)

Side 1 Signal	Connector C L/H	Connector C Pin	Connector C Pin	Connector C L/H	Side 2 Signal
NOT USED		1	2		NOT USED
0V		3	4		0V
WDP	L	5	6	L	SWDP
TAD00	L	7	8	L	FAD
NOT USED		9	10	L	TAD01
ST06 LATCH	L	11	12		NOT USED
STC	L	13	14	L	ST03 LATCH
ST10 LATCH	L	15	16	L	ST02 LATCH
BLK LTH	L	17	18	L	ST15 LATCH
SWD03	L	19	20	L	SWD02
SWD05	L	21	22	L	SWD04
SWD07	L	23	24	L	SWD00
SWD01	L	25	26	L	SWD06
LWD	L	27	28		NOT USED
ROMPS	H	29	30	H	OVRNS
ERMX05	H	31	32	H	ERMX04
BUS PE	H	33	34	H	ERMXP
ERMX07	H	35	36	H	ERMX06
ERMX03	H	37	38	H	ERMX02
ERMX01	H	39	40	H	ERMX00
0V		41	42		0V
0V		43	44		0V
UBUS ACLO	L	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50		NOT USED
0V		51	52		0V
0V		53	54		0V
ST07	L	55	56	L	ST06
ST10	L	57	58	L	ST11
ST09	L	59	60	L	ST00
ST08	L	61	62	L	ST15
BLOCK	L	63	64	L	ST13
ST12	L	65	66	L	ST02
ST03	L	67	68	L	ST14
ST01	L	69	70	L	ST04
ST05	L	71	72	L	FBSY
NOT USED		73	74		NOT USED
RD03	L	75	76	L	RD05
RD02	L	77	78	L	RD07
RD04	L	79	80	L	RD06
END ST	L	81	82	L	RD01
RD00	L	83	84	L	RDP
NOT USED		85	86	L	RSTR
NOT USED		87	88	L	WSTR
NOT USED		89	90	H	TREQ
NOT USED		91	92		0V
UBUS DCLO	L	93	94		NOT USED

8.4 V-MASTER/780 SBI PIN/SIGNALS

Table 8-4 lists pin/signal assignments for the 12 SBI connectors. The L/H column indicates the asserted (active) state of the signal; L = Low and H = High.

Table 8-4. Pin/Signal Assignments, SBI Connectors

Connector	Pin	L/H	Signal Name	Pin	Connector
J1	A		GROUND	B	J7
J1	B	L	BUS SBI B00	A	J7
J1	C		GROUND	D	J7
J1	D	L	BUS SBI B01	C	J7
J1	E		GROUND	F	J7
J1	F		GROUND	E	J7
J1	H		GROUND	J	J7
J1	J	L	BUS SBI B02	H	J7
J1	K		GROUND	L	J7
J1	L		GROUND	K	J7
J1	M		(NOT USED)	N	J7
J1	N		(NOT USED)	M	J7
J1	P		GROUND	R	J7
J1	R	L	BUS SBI B03	P	J7
J1	S		GROUND	T	J7
J1	T		GROUND	S	J7
J1	U		GROUND	V	J7
J1	V		GROUND	U	J7
J1	W		GROUND	X	J7
J1	X		GROUND	W	J7
J1	Y		GROUND	Z	J7
J1	Z		GROUND	Y	J7
J1	AA		GROUND	BB	J7
J1	BB	L	BUS SBI B04	AA	J7
J1	CC		GROUND	DD	J7
J1	DD	L	BUS SBI B07	CC	J7
J1	EE		GROUND	FF	J7
J1	FF	L	BUS SBI B05	EE	J7
J1	HH		GROUND	JJ	J7
J1	JJ		GROUND	HH	J7
J1	KK		GROUND	LL	J7
J1	LL	L	BUS SBI B08	KK	J7
J1	MM		GROUND	NN	J7
J1	NN	L	BUS SBI B06	MM	J7
J1	PP		GROUND	RR	J7
J1	RR	L	BUS SBI B09	PP	J7
J1	SS		GROUND	TT	J7
J1	TT	L	BUS SBI B10	SS	J7
J1	UU		GROUND	VV	J7
J1	VV	L	BUS SBI B11	UU	J7

Table 8-4. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J2	A		GROUND	B	J8
J2	B		(NOT USED)	A	J8
J2	C		GROUND	D	J8
J2	D		(NOT USED)	C	J8
J2	E		GROUND	F	J8
J2	F		GROUND	E	J8
J2	H		GROUND	J	J8
J2	J		GROUND	H	J8
J2	K		GROUND	L	J8
J2	L	L	BUS SBI B12	K	J8
J2	M		GROUND	N	J8
J2	N	L	BUS SBI B14	M	J8
J2	P		GROUND	R	J8
J2	R		GROUND	P	J8
J2	S		GROUND	T	J8
J2	T	L	BUS SBI B13	S	J8
J2	U		GROUND	V	J8
J2	V		GROUND	U	J8
J2	W		GROUND	X	J8
J2	X	L	BUS SBI B15	W	J8
J2	Y		GROUND	Z	J8
J2	Z		GROUND	Y	J8
J2	AA		GROUND	BB	J8
J2	BB		GROUND	AA	J8
J2	CC		GROUND	DD	J8
J2	DD		GROUND	CC	J8
J2	EE		GROUND	FF	J8
J2	FF		GROUND	EE	J8
J2	HH		GROUND	JJ	J8
J2	JJ	L	BUS SBI B16	HH	J8
J2	KK		GROUND	LL	J8
J2	LL		GROUND	KK	J8
J2	MM		GROUND	NN	J8
J2	NN		GROUND	MM	J8
J2	PP		GROUND	RR	J8
J2	RR	L	BUS SBI B17	PP	J8
J2	SS		GROUND	TT	J8
J2	TT	L	BUS SBI B18	SS	J8
J2	UU		GROUND	VV	J8
J2	VV	L	BUS SBI B19	UU	J8

Table 8-4. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J3	A		GROUND	B	J9
J3	B		GROUND	A	J9
J3	C		GROUND	D	J9
J3	D	L	BUS SBI B20	C	J9
J3	E		GROUND	F	J9
J3	F	L	BUS SBI B23	E	J9
J3	H		GROUND	J	J9
J3	J	L	BUS SBI B21	H	J9
J3	K		GROUND	L	J9
J3	L		GROUND	K	J9
J3	M		GROUND	N	J9
J3	N	L	BUS SBI B22	M	J9
J3	P		GROUND	R	J9
J3	R		GROUND	P	J9
J3	S		GROUND	T	J9
J3	T		GROUND	S	J9
J3	U		GROUND	V	J9
J3	V		GROUND	U	J9
J3	W		GROUND	X	J9
J3	X		GROUND	W	J9
J3	Y		GROUND	Z	J9
J3	Z		GROUND	Y	J9
J3	AA		GROUND	BB	J9
J3	BB	L	BUS SBI B24	AA	J9
J3	CC		GROUND	DD	J9
J3	DD	L	BUS SBI B27	CC	J9
J3	EE		GROUND	FF	J9
J3	FF	L	BUS SBI B25	EE	J9
J3	HH		GROUND	JJ	J9
J3	JJ	L	BUS SBI B28	HH	J9
J3	KK		GROUND	LL	J9
J3	LL	L	BUS SBI B26	KK	J9
J3	MM		GROUND	NN	J9
J3	NN	L	BUS SBI B29	MM	J9
J3	PP		GROUND	RR	J9
J3	RR	L	BUS SBI B30	PP	J9
J3	SS		GROUND	TT	J9
J3	TT	L	BUS SBI FAIL	SS	J9
J3	UU		GROUND	VV	J9
J3	VV	L	BUS SBI B31	UU	J9

Table 8-4. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J4	A		GROUND	B	J10
J4	B	L	BUS SBI M0	A	J10
J4	C		GROUND	D	J10
J4	D	L	BUS SBI DEAD	C	J10
J4	E		GROUND	F	J10
J4	F	L	BUS SBI M1	E	J10
J4	H		GROUND	J	J10
J4	J	L	BUS SBI M2	H	J10
J4	K		GROUND	L	J10
J4	L	L	BUS SBI M3	K	J10
J4	M		GROUND	N	J10
J4	N	L	BUS SBI P0	M	J10
J4	P		GROUND	R	J10
J4	R	L	BUS SBI SPARE 0	P	J10
J4	S		GROUND	T	J10
J4	T	L	BUS SBI P1	S	J10
J4	U		GROUND	V	J10
J4	V		GROUND	U	J10
J4	W		GROUND	X	J10
J4	X		GROUND	W	J10
J4	Y		GROUND	Z	J10
J4	Z	L	BUS SBI SPARE 1	Y	J10
J4	AA		GROUND	BB	J10
J4	BB	L	BUS SBI TAG 0	AA	J10
J4	CC		GROUND	DD	J10
J4	DD	L	BUS SBI ID0	CC	J10
J4	EE		GROUND	FF	J10
J4	FF	L	BUS SBI TAG 1	EE	J10
J4	HH		GROUND	JJ	J10
J4	JJ		GROUND	HH	J10
J4	KK		GROUND	LL	J10
J4	LL	L	BUS SBI ID1	KK	J10
J4	MM		GROUND	NN	J10
J4	NN	L	BUS SBI TAG 2	MM	J10
J4	PP		GROUND	RR	J10
J4	RR	L	BUS SBI ID2	PP	J10
J4	SS		GROUND	TT	J10
J4	TT	L	BUS SBI ID3	SS	J10
J4	UU		GROUND	VV	J10
J4	VV	L	BUS SBI ID4	UU	J10

Table 8-4. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J5	A		GROUND	B	J11
J5	B	L	BUS SBI REQ 4	A	J11
J5	C		GROUND	D	J11
J5	D	L	BUS SBI REQ 7	C	J11
J5	E		GROUND	F	J11
J5	F	L	BUS SBI REQ 5	E	J11
J5	H		GROUND	J	J11
J5	J	L	BUS SBI TP	H	J11
J5	K		GROUND	L	J11
J5	L		GROUND	K	J11
J5	M		GROUND	N	J11
J5	N	L	BUS SBI REQ 6	M	J11
J5	P		GROUND	R	J11
J5	R	H	BUS SBI P CLK	P	J11
J5	S		GROUND	T	J11
J5	T	H	BUS SBI TP	S	J11
J5	U		GROUND	V	J11
J5	V		GROUND	U	J11
J5	W		GROUND	X	J11
J5	X	H	BUS SBI PD CLK	W	J11
J5	Y		GROUND	Z	J11
J5	Z	L	BUS SBI P CLK	Y	J11
J5	AA		GROUND	BB	J11
J5	BB	L	BUS SBI PD CLK	AA	J11
J5	CC		GROUND	DD	J11
J5	DD	L	BUS SBI MP2	CC	J11
J5	EE		GROUND	FF	J11
J5	FF	L	BUS SBI MP1	EE	J11
J5	HH		GROUND	JJ	J11
J5	JJ		GROUND	HH	J11
J5	KK		GROUND	LL	J11
J5	LL	L	SBI BUS ALERT	KK	J11
J5	MM		GROUND	NN	J11
J5	NN	L	SBI BUS UNJAM	MM	J11
J5	PP		GROUND	RR	J11
J5	RR	L	BUS SBI CNF 0	PP	J11
J5	SS		GROUND	TT	J11
J5	TT	L	BUS SBI FAULT	SS	J11
J5	UU		GROUND	VV	J11
J5	VV	L	BUS SBI CNF 1	UU	J11

Table 8-4. Pin/Signal Assignments, SBI Connectors (continued)

Connector	Pin	L/H	Signal Name	Pin	Connector
J6	A		GROUND	B	J12
J6	B	L	BUS SBI INTLK	A	J12
J6	C		GROUND	D	J12
J6	D	L	BUS SBI TR01	C	J12
J6	E		GROUND	F	J12
J6	F	L	BUS SBI TR00	E	J12
J6	H		GROUND	J	J12
J6	J	L	BUS SBI TR03	H	J12
J6	K		GROUND	L	J12
J6	L	L	BUS SBI TR02	K	J12
J6	M		GROUND	N	J12
J6	N	L	BUS SBI TR04	M	J12
J6	P		GROUND	R	J12
J6	R		GROUND	P	J12
J6	S		GROUND	T	J12
J6	T	L	BUS SBI TR05	S	J12
J6	U		GROUND	V	J12
J6	V	L	BUS SBI TR06	U	J12
J6	W		GROUND	X	J12
J6	X	L	BUS SBI TR07	W	J12
J6	Y		GROUND	Z	J12
J6	Z	L	BUS SBI TR08	Y	J12
J6	AA		GROUND	BB	J12
J6	BB		GROUND	AA	J12
J6	CC		GROUND	DD	J12
J6	DD	L	BUS SBI TR09	CC	J12
J6	EE		GROUND	FF	J12
J6	FF	L	BUS SBI TR10	EE	J12
J6	HH		GROUND	JJ	J12
J6	JJ	L	BUS SBI TR11	HH	J12
J6	KK		GROUND	LL	J12
J6	LL	L	BUS SBI TR13	KK	J12
J6	MM		GROUND	NN	J12
J6	NN		GROUND	MM	J12
J6	PP		GROUND	RR	J12
J6	RR	L	BUS SBI TR12	PP	J12
J6	SS		GROUND	TT	J12
J6	TT	L	BUS SBI TR14	SS	J12
J6	UU		GROUND	VV	J12
J6	VV	L	BUS SBI TR15	UU	J12

8.5 BUS INTERFACE PCBA PIN/SIGNALS

Table 8-5 lists pin/signal assignments for the Bus Interface PCBA edge connectors.

NOTE

Edge connectors on all plug-in PCBAs have odd-numbered pins on the component side (side 1) and even-numbered pins on the solder side (side 2).

Table 8-5. Pin/Signal Assignments, Bus Interface PCBA

Side 1 Signal	Connector A L/H	Connector A Pin	Connector A Pin	Connector A L/H	Side 2 Signal
INTERRUPT ODD	H	1	2	H	INTERRUPT EVEN
TWO CHANNEL	L	3	4	L	BUS SBI B00
NOT USED		5	6	L	BUS SBI B01
NOT USED		7	8		NOT USED
NOT USED		9	10	L	BUS SBI B02
NOT USED		11	12		NOT USED
BUS MBA INT B00	H	13	14		NOT USED
NOT USED		15	16	L	BUS SBI B03
BUS MBA INT B01	H	17	18	H	BUS MBA INT B02
BUS MBA INT B03	H	19	20		+5V
BUS MBA INT B04	H	21	22	H	BUS MBA INT B05
GND		23	24		GND
BUS MBA INT B06	H	25	26	L	BUS SBI B04
BUS MBA INT B07	H	27	28	L	BUS SBI B07
HOLD TR	H	29	30	L	BUS SBI B05
SEND TR	H	31	32	L	BUS SBI B08
SEND TR HOLD	H	33	34	L	BUS SBI B06
BUS MBA INT B08	H	35	36	L	BUS SBI B09
BUS MBA INT B09	H	37	38		+5V
NOT USED		39	40	L	BUS SBI B10
NOT USED		41	42	L	BUS SBI B11
GND		43	44		GND
BUS MBA INT B10	H	45	46	H	BUS MBA INT B11
NOT USED		47	48		NOT USED
NOT USED		49	50		NOT USED
GND		51	52		GND
TS0	L	53	54		NOT USED
NOT USED		55	56		NOT USED
NOT USED		57	58		+5V
BUS MBA INT B12	H	59	60	H	BUS MBA INT B13
BUS MBA INT B14	H	61	62	H	BUS MBA INT B15
TR SEL A	H	63	64	L	BUS SBI B12
TR SEL B	H	65	66	L	BUS SBI B14
TR SEL C	H	67	68		NOT USED
NOT USED		69	70	L	BUS SBI B13
GND		71	72		GND
NOT USED		73	74	L	BUS SBI B15
NOT USED		75	76		+5V
BUS MBA INT B16	H	77	78	H	BUS MBA INT B17
NOT USED		79	80		NOT USED
BUS MBA INT B18		81	82	H	BUS MBA INT B19

Table 8-5. Pin/Signal Assignments, Bus Interface PCBA (continued)

Side 1 Signal	Connector A L/H	Pin	Pin	L/H	Side 2 Signal
BUS MBA INT B20	H	83	84		NOT USED
NOT USED		85	86	L	BUS SBI B16
TR SEL D	H	87	88		NOT USED
NOT USED		89	90	L	BUS SBI B17
BUS MBA INT B21	H	91	92	L	BUS SBI B18
BUS MBA INT B22	H	93	94	L	BUS SBI B19
Side 1 Signal	**Connector B L/H**	**Pin**	**Pin**	**L/H**	**Side 2 Signal**
NOT USED		1	2	H	BUS MBA INT B23
NOT USED		3	4	L	BUS SBI B20
NOT USED		5	6	L	BUS SBI B23
NOT USED		7	8	L	BUS SBI B21
NOT USED		9	10		NOT USED
NOT USED		11	12	L	BUS SBI B22
NOT USED		13	14		NOT USED
NOT USED		15	16		NOT USED
NOT USED		17	18		NOT USED
GEN MAP PAR	H	19	20		+5V
NOT USED		21	22	L	BUS SBI B24
GND		23	24		GND
NOT USED		25	26	L	BUS SBI B27
PGM INIT	L	27	28	L	BUS SBI B25
PWRF INIT	L	29	30	L	BUS SBI B28
NOT USED		31	32	L	BUS SBI B26
SET PGE	L	33	34	L	BUS SBI B29
NOT USED		35	36	L	BUS SBI B30
NOT USED		37	38		+5V
NOT USED		39	40	L	BUS SBI B31
CLK EXT CMD	H	41	42		NOT USED
GND		43	44		GND
CLK EXT READ	H	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50	H	BUS MBA INT B24
GND		51	52		GND
BUS MBA INT B25	H	53	54	H	BUS MBA INT B26
BUS MBA INT B27	H	55	56	H	BUS MBA INT B28
BUS MBA INT B29	H	57	58	H	BUS MBA INT B30
BUS MBA INT B31	H	59	60	L	BUS SBI M0
WRITE FCN	H	61	62	L	BUS SBI M1
NOT USED		63	64	L	BUS SBI M3
NOT USED		65	66	L	BUS SBI M2
NOT USED		67	68	L	BUS SBI P0
NOT USED		69	70		NOT USED
GND		71	72		GND
RMW FCN	H	73	74	L	BUS SBI P1
EXP WD	H	75	76	H	EX OP DONE

Table 8-5. Pin/Signal Assignments, Bus interface PCBA (continued)

Side 1 Signal	Connector B L/H	Pin	Pin	L/H	Side 2 Signal
CLK VALID CMD	H	77	78	L	BUS SBI TAG 0
REC FAULT	L	79	80	H	BUS SBI ID0
NOT USED		81	82	L	BUS SBI TAG 1
NOT USED		83	84	L	BUS SBI ID1
STORED SBI B11	H	85	86	L	BUS SBI TAG 2
+5V		87	88	L	BUS SBI ID2
SET 1S TIMEOUT	L	89	90	L	BUS SBI ID3
SET RD TIMEOUT B	L	91	92	L	BUS SBI ID4
SET RD TIMEOUT A	L	93	94	L	WRITE DATA
Side 1 Signal	**Connector C L/H**	**Pin**	**Pin**	**L/H**	**Side 2 Signal**
ARB CK	L	1	2	L	BUS SBI REQ 4
NOT USED		3	4	L	BUS SBI REQ 7
UNEXP RD FLT	H	5	6	L	BUS SBI REQ 5
INTERRUPT CPU	L	7	8	L	BUS SBI TP
MULTI XMIT FLT	H	9	10	H	ID0 STORED
WRITE SEQ FLT	H	11	12	L	BUS SBI REQ 6
XMITTED FLT	H	13	14	H	BUS SBI PCLK
RD ADR	H	15	16	H	BUS SBI TP
DT READ	H	17	18	H	INT RD REQ
NOT USED		19	20	H	BUS SBI PDCLK
CMD REQ	L	21	22	L	BUS SBI PCLK
GND		23	24		GND
PARITY FLT	H	25	26	L	BUS SBI PDCLK
SET CORRECT RD	L	27	28	H	CLK DIB 2
CLK DIB 1	H	29	30	L	SET RD SUB
ENAB WDE MUX	H	31	32	L	SET CMD READY
NOT USED		33	34	L	BUS SBI UNJAM
INIT COND	L	35	36	L	BUS SBI CONF0
NOT USED		37	38	L	BUS SBI FAULT
INT DIF T1 CLK	L	39	40	L	BUS SBI CONF1
UNJAM	L	41	42	H	INT BUS 0 CLK
GND		43	44		GND
NOT USED		45	46		+5V
INT DIF T1 CLK	L	47	48	L	RD PEND A
INT DIF T3 CLK	L	49	50	H	INT DIF T3 CLK
GND		51	52		GND
INT BUS 1 CLK	L	53	54	L	CHNL ADR
INT DIF T0 CLK	L	55	56	H	INT DIF T0 CLK
INT DIF T2 CLK	L	57	58		NOT USED
INT DIF T2 CLK	H	59	60		NOT USED
BYTE MASK 1-0	H	61	62		NOT USED
BYTE MASK 1-2	H	63	64		NOT USED
BYTE MASK 1-1	H	65	66		NOT USED
NOT USED		67	68		NOT USED
BYTE MASK 1-3	H	69	70		NOT USED

Table 8-5. Pin/Signal Assignments, Bus Interface PCBA (continued)

Side 1 Signal	Connector C L/H	Pin	Pin	L/H	Side 2 Signal
GND		71	72		GND
DT GO	L	73	74	H	BYTE MASK 2-2
BYTE MASK 2-3	H	75	76	H	BYTE MASK 2-1
BYTE MASK 2-0	H	77	78		NOT USED
-5.2V		79	80	H	STROBE MAP
NOT USED		81	82		-5.2V
NOT USED		83	84		NOT USED
SET ERROR CNF	L	85	86	L	REQ COMPLETE
SET N/R CNF	L	87	88		NOT USED
+5V PS DCLO	H	89	90	H	-5V PS DCLO
+5V PS ACLO	H	91	92	H	-5V PS ACLO
WD2 ACK	H	93	94	H	ENAB WD1 MUX

8.6 BUS TRANSLATOR PCBA PIN/SIGNALS

Table 8-6 lists pin/signal assignments for the Bus Translator PCBA edge connectors.

Table 8-6. Pin/Signal Assignments, Bus Translator PCBA

Side 1 Signal	Connector A L/H	Pin	Pin	L/H	Side 2 Signal
INTERRUPT ODD	H	1	2	H	INTERRUPT EVEN
TWP CHNL	L	3	4		NOT USED
NOT USED		5	6		NOT USED
NOT USED		7	8		NOT USED
B PRESENT	L	9	10	L	A PRESENT
NOT USED		11	12		NOT USED
BUS MBA INIT B00	H	13	14		NOT USED
NOT USED		15	16		NOT USED
BUS MBA INT B01	H	17	18	H	BUS MBA INT B02
BUS MBA INT B03	H	19	20		+5V
BUS MBA INT B04	H	21	22	H	BUS MBA INT B05
GND		23	24		GND
BUS MBA INT B06	H	25	26		NOT USED
BUS MBA INT B07	H	27	28		NOT USED
HOLD TR	H	29	30		NOT USED
SEND TR	H	31	32		NOT USED
SEND TR HOLD	H	33	34		NOT USED
BUS MBA INT B08	H	35	36		NOT USED
BUS MBA INT B09	H	37	38		+5V
CLR B	H	39	40	H	CLR A
DMA EN B	H	41	42	H	DMA EN A
GND		43	44		GND
BUS MBA INT B10	H	45	46	H	BUS MBA INT B11
780 ST B	L	47	48	L	780 ST A

Table 8-6. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1 Signal	Connector A L/H	Pin	Pin	L/H	Side 2 Signal
DMA READ B	H	49	50	H	DMA READ A
GND		51	52		GND
DMA SEL B	L	53	54		NOT USED
MBA SEL 0 B	L	55	56	L	MBA SEL 0 A
NOT USED		57	58		+5V
BUS MBA INT B12	H	59	60	H	BUS MBA INT B13
BUS MBA INT B14	H	61	62		NOT USED
TR SEL A	H	63	64		NOT USED
TR SEL B	H	65	66		NOT USED
TR SEL C	H	67	68		NOT USED
BG5 IN B	H	69	70	H	BG5 IN A
GND		71	72		GND
NOT USED		73	74		NOT USED
NOT USED		75	76		+5V
BUS MBA INT B16	H	77	78	H	BUS MBA INT B17
BUS BR5 B	L	79	80	L	BUS BR5 A
BUS MBA INT B18	H	81	82	H	BUS MBA INT B19
BUS MBA INT B20	H	83	84	L	ARB 1
ARB 2	L	85	86	L	ARB 3
ARB 4	L	87	88	L	ARB 5
ARB 6	L	89	90	L	ARB 7
BUS MBA INT B21	H	91	92	L	CMI HOLD
BUS MBA INT B22	H	93	94		NOT USED

Side 1 Signal	Connector B L/H	Pin	Pin	L/H	Side 2 Signal
CMI DATA B00	H	1	2	H	BUS MBA INT B23
CMI DATA B01	H	3	4	H	CMI DATA B02
CMI DATA B03	H	5	6	H	CMI DATA B04
CMI DATA B05	H	7	8	H	CMI DATA B06
CMI DATA B07	H	9	10	H	CMI DATA B08
NOT USED		11	12	H	CMI DATA B09
CMI DATA B10	H	13	14	H	CMI DATA B11
CMI DATA B12	H	15	16	H	CMI DATA B13
CMI DATA B14	H	17	18	H	CMI DATA B15
CMI DATA B16	H	19	20		+5V
CMI DATA B17	H	21	22	H	CMI DATA B18
GND		23	24		NOT USED
CMI DATA B19	H	25	26	H	CMI DATA B20
CMI DATA B21	H	27	28	H	CMI DATA B22
PWRF INIT	L	29	30	H	CMI DATA B23
CMI DATA B24	H	31	32	H	CMI DATA B25
CMI DATA B26	H	33	34	H	CMI DATA B27
CMI DATA B28	H	35	36	H	CMI DATA B29
CMI DATA B30	H	37	38		+5V
CMI DATA B31	H	39	40	L	CMI STATUS 00
CMI STATUS 01	L	41	42	L	CMI DBB2

Table 8-6. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1 Signal	Connector B L/H	Pin	Pin	L/H	Side 2 Signal
GND		43	44		GND
CMI B CLK	L	45	46		+5V
NOT USED		47	48		NOT USED
NOT USED		49	50	H	BUS MBA INT B24
GND		51	52		GND
BUS MBA INT B25	H	53	54	H	BUS MBA INT B26
BUS MBA INT B27	H	55	56	H	BUS MBA INT B28
BUS MBA INT B29	H	57	58	H	BUS MBA INT B30
BUS MBA INT B31	H	59	60	L	BUS SBI DEAD
WRITE FCN	H	61	62		NOT USED
NOT USED		63	65		NOT USED
NOT USED		65	66		NOT USED
NOT USED		67	68		NOT USED
NOT USED		69	70		NOT USED
GND		71	72		GND
NOT USED		73	74		NOT USED
EXP WD	H	75	76	H	EXT OP DONE + TO
CLK VALID CMD	H	77	78		NOT USED
REC FAULT	L	79	80		NOT USED
NOT USED		81	82		NOT USED
NOT USED		83	84		NOT USED
STORED SBI B11	H	85	86		NOT USED
+5V		87	88		NOT USED
SET IS TIMEOUT	L	89	90		NOT USED
SET RD TIMEOUT B	L	91	92		NOT USED
SET RD TIMEOUT A	L	93	94		NOT USED

Side 1 Signal	Connector C L/H	Pin	Pin	L/H	Side 2 Signal
ARB OK	L	1	2		NOT USED
NOT USED		3	4		NOT USED
UNEXP RD FLT	H	5	6		NOT USED
INTERRUPT CPU	L	7	8		NOT USED
MULTI XMIT FLT	H	9	10	H	ID0 STORED
WRITE SEQ FLT	H	11	12		NOT USED
XMITTED FLT	H	13	14		NOT USED
RD ADR	H	15	16		NOT USED
DT READ	H	17	18		NOT USED
NOT USED		19	20		NOT USED
CMD REG	L	21	22		NOT USED
GND		23	24		GND
PARITY FLT	H	25	26		NOT USED
SET CORRECT RD	L	27	28	H	CLK DIB 2
CLK DTB 1	H	29	30	L	SET RD SUB
ENAB WDE MUX	H	31	32	L	SET CMD READY
NOT USED		33	34		NOT USED
INIT COND	L	35	36		NOT USED

Table 8-6. Pin/Signal Assignments, Bus Translator PCBA (continued)

Side 1 Signal	Connector C L/H	Pin	Pin	L/H	Side 2 Signal
NOT USED		37	38		NOT USED
INT DIF T1 CLK	L	39	40		NOT USED
UNJAM	L	41	42	H	INT BUS 0 CLK
GND		43	44		GND
UBUS ALCO	L	45	46		+5V
INT DIF T1 CLK	H	47	48		NOT USED
INT DIF T3 CLK	L	49	50	H	INT DIF T3 CLK
GND		51	52		GND
INT BUS CLK	L	53	54	L	CHNL ADR
INT DIF T0 CLK	L	55	56	H	INT DIF T0 CLK
INT DIF T2 CLK	H	57	58	L	BUS SBI TR01
INT DIF T2 CLK	L	59	60	L	BUS SBI TR00
BYTE MASK 1-0	H	61	62	L	BUS SBI TR03
BYTE MASK 1-2	H	63	64	L	BUS SBI TR02
BYTE MASK 1-1	H	65	66	L	BUS SBI TR04
NOT USED		67	68	L	BUS SBI TR05
BYTE MASK 1-3	H	69	70	L	BUS SBI TR06
GND		71	72		GND
BYTE MASK 2-2	H	73	74	L	BUS SBI TR07
BYTE MASK 2-3	H	75	76	L	BUS SBI TR08
BYTE MASK 2-0	H	77	78	H	BYTE MASK 2-1
-5.2V		79	80	L	BUS SBI TR09
NOT USED		81	82	L	BUS SBI TR10
NOT USED		83	84	L	BUS SBI TR11
SET ERROR CNF	L	85	86	L	REQ COMPLETE
SET N/R CNF	L	87	88		NOT USED
+5V PS DCLO	H	89	90	H	-5V PS DCLO
+5V PS ACLO	H	91	92	H	-5V PS ACLO
UBUS DCLO	L	93	94	H	ENAB WD1 MUX

Appendix A
TC7000 TAPE COUPLER CONFIGURATION AND OPTION SELECTION

A.1 OVERVIEW

To allow the user of the TC7000 Tape Coupler the greatest flexibility in selecting tape transports for the DEC VAX-11/750 or VAX/VMS-11/780 computer system, the TC7000 Tape Coupler supports a wide variety of tape transport configurations, and provides the means for selecting other options. This appendix is intended to be a quick reference to the various tape transport models and to the various switch settings on the TC7000 Tape Coupler that make such flexibility possible. This appendix is divided into three subsections, as listed in the following table:

Subsection	Title
A.1	Overview
A.2	Tape Transport Models
A.3	Configuration Switches

A.2 TAPE TRANSPORT MODELS

The TC7000 Tape Coupler can control a wide variety of tape transport models that use nine-track, 1/2-inch wide tape, that are compatible with Pertec or STC interfaces, and that operate in various data density modes at various tape speeds. Appendix B lists tape transport models that are currently supported by the TC7000 Tape Coupler plus switch settings and jumper connections for configuring those tape transports.

A.3 CONFIGURATION SWITCHES

The TC7000 Tape Coupler PCBA contains five DIP switch packs (SW1, SW2, SW3, SW4, and SW5) that can be used to configure the TC7000 Tape Coupler for compatibility with system tape transports and to select various options. Switch positions shown in the tables of this Appendix reflect the functions as defined in Revision C firmware.

Switch SW1 has 10 switches, whose functions are listed and described in Table A-1.

NOTE

All switches listed in this appendix are assumed to be normally closed for described option or function to be selected.

Table A-1. DIP Switch SW1 Functions

Number of Tape Transports	SW1-3	SW1-2	SW1-1
1	Open	Open	Open
2	Open	Open	Closed
3	Open	Closed	Open
4	Open	Closed	Closed
5	Closed	Open	Open
6	Closed	Open	Closed
7	Closed	Closed	Open
8	Closed	Closed	Closed

Switch	Closed	Open	Function	Interface
SW1-4	Enable	Disable	Reset Density Select Line	Pertec
SW1-5	Enable	Disable	CDC 92185 Drive Select.[1] Converts Pertec Read Reverse to Space Reverse.[2] Required for all non-buffered CDC drives.	Pertec
SW1-6	Enable	Disable	Invert Density Select Line	Pertec
SW1-7	Enable	Disable	Latched EOT Status - Odd	Pertec
SW1-8	Enable	Disable	Latched EOT Status - Even	Pertec
SW1-4	---	---	Not Used	STC
SW1-5	Enable	Disable	Software Tri-Density Select[3]	STC
SW1-6	Enable	Disable	Change NRZI to GCR Select	STC
SW1-7	Enable	Disable	Latched EOT Status - Odd	STC
SW1-8	Enable	Disable	Latched EOT Status - Even	STC
SW1-9	STC	Pertec	Interface Select	Common
SW1-10	4K	2K	PROM Size Select[4]	Common

[1] SW1-5 and SW3-2 both ON enable the Kennedy 9600 remote density select.
[2] SW3-3 must be ON to enable this feature.
[3] **Only** supports STC TRI-DENSITY tape transport with patched TMDRIVER.
[4] MUST BE ON for Rev C and later Data PROMs.

Table A-2. DIP Switch SW2 Functions

Switch	Closed	Open	Function	Interface
SW2-1	Enable	Disable	For transport needs 50 microseconds to assert REWS and RDYS during rewind[1]	Pertec
SW2-2	--	--	Not Used[2]	
SW2-3	--	--	Not Used[2]	
SW2-4	--	--	Not Used[2]	

[1]Currently supports TELEX 9250 only.
[2]Unused switches must be OFF.

Table A-3. DIP Switch SW3 Functions

Switch	Closed	Open	Function	Interface
SW3-1	Enable	Disable (Normal Condition)	Hard Reset Condition	Common
SW3-2	Enable	Disable	Cipher M990 remote density[1]	Pertec
SW3-3	Enable	Disable	Alter READ REVERSE and WRITE CHECK REVERSE into SPACE REVERSE	Pertec
SW3-4	Enable	Disable	2 START pulses at BOT	Pertec only

[1]SW3-2 and SW1-5 both ON enable Kennedy 9600 remote density select.

Table A-4. DIP Switch SW4 Functions

Switch	Closed	Open	Function
SW4-1	---	---	Not used[1]
SW4-2	---	---	Not used[1]
SW4-3	---	---	Not used[1]
SW4-4	---	---	Not used[1]
SW4-5	---	---	Not used[1]
SW4-6	Disable	Enable	Blank Tape Timer[2]
SW4-7	VAX-11/780	VAX-11/750	CPU Select
SW4-8	Enable	Disable	Density Check Select

[1]Unused switches MUST BE open (OFF).
[2]Revision D and later PROMs only.

Switch pack SW5 has eight switches, whose functions are listed and described in Table A-5 (See sections 4.4 and 4.5 for proper configuration in the VAX-11/750 and V-MASTER VAX-11/780 systems.

Table A-5. DIP Switch SW5 Functions

Switch	Function
SW5-1	Selects one-shot enable (set in VAX-11/780 only).
SW5-2 SW5-3 SW5-4 SW5-5 SW5-6	SW5-2 through SW5-6 are used to provide the code that selects the arbitration level (CMI/VMI Bus priority) as described in subsection 4.5. The selection codes are listed in Table A-6.
SW5-7 SW5-8	SW5-7 and SW5-8 are used to provide the code that selects the Base Address, Interrupt Vector Address, and MBA Device Number for the VAX-11/750 CPU as described in subsection 4.4. The selection codes are listed in Table A-7. These switches are also used to distinguish the two slots in the V-MASTER which accommodate the TC7000 Tape Coupler PCBA (see subsection 4.5.1).

Table A-6. Arbitration Level Selection

Level	DIP Switch SW5- 2	3	4	5	6	Rank
3	C	O	O	O	O	Highest MBA level
2	O	C	O	C	O	
1	O	O	C	C	C	Lowest MBA level
O = open, C = closed						

Table A-7. Base Address, Interrupt Vector Address, and MBA Device Number Selection

Switch SW5-7	SW5-8	Base Address	Interrupt Vector Address	MBA Device Number
O	O	F28000	150	RH0
O	C	F2A000	154	RH1
C	O	F2C000	158	RH2
O = open, C = Closed				

Appendix B
SPECIFIC CONFIGURATIONS

B.1 OVERVIEW

This appendix contains configuration information for positioning jumpers and setting configuration option switches for specific tape transports supported by the TC7000 Tape Coupler. This appendix is divided into six subsections as listed in the following table:

Subsection	Title
B.1	Overview
B.2	CDC 92181
B.3	CDC 92185
B.4	Kennedy 9400
B.5	STC 1935/1950
B.6	STC2920
B.7	Cipher M990
B.8	TELEX 9250

B.2 CDC 92181

The CDC 92181 tape transport is PE-only, dual-speed 25/100 ips with Pertec interface. It uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard Connector
P4	J1
P5	J2

The tape transport contains a DIP switch pack with four DIP switches for address selection. This DIP switch pack is located at coordinates 21D on the Formatter/Control PCBA near test point two (TP2). Switches in this DIP switch pack should be set as listed in the following table:

Switch	Function	Setting
1	Formatter Address	OFF
2	Tape Transport Address	OFF
3	Tape Transport Address	OFF
4	Not Used	OFF

Address settings for these switches are for Unit 0. Below the DIP switches are four jumper plugs which should be positioned in the following locations:

Plug	Position	Function
W1	1 to 2	Channel Parity Check
W3	2 to 3	Fixed/Variable Short Gaps
W4	2 to 3	Fixed/Variable Long Gaps
W5	2 to 3	Automatic Velocity Select[1]

[1]In this mode, the tape transport selects the fastest velocity mode it can maintain consistently; i.e., 25 ips start/stop, 25 ips streaming, or 100 ips streaming. Software selection of NRZI mode overrides the automatic velocity control of the tape transport and forces it to the 100 ips streaming mode unless switch SW1-4 is closed (ON).

Also on the Formatter/Control PCBA for this tape transport, two terminator resistor packs must be installed at locations G18 and H25.

The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch	DIP Switch Pack SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	ON	OFF	OFF	OFF	through
5	OFF			OFF	A-7
6	OFF			OFF	
7	ON[2]			X[3]	
8	ON[4]			OFF	
9	OFF				
10	ON				

[1]See Appendix A, Table A-1.
[2]ON if odd-numbered tape transport.
[3]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[4]ON if even-numbered tape transport.

B.3 CDC 92185

The CDC 92185 tape transport is PE/GCR, dual-speed 25/75 ips with Pertec interface. It does not support read reverse. It uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard Connector
J2	J1
J3	J2

The tape transport contains a DIP switch pack with four DIP switches for address selection. This DIP switch pack is located at coordinates F4 on the Interface PCBA. Switches in this DIP switch pack should be set as listed in the following table:

Switch	Function	Setting
1	Formatter Address	OFF
2	Transport Address 1	OFF
3	Transport Address 0	OFF
4	Not Used	OFF

Address settings for these switches are for Unit 0. Near the DIP switches, at coordinates D9 on the Interface PCBA are five jumper plugs which should be positioned in the following locations:

Plug	Position	Function
W1	2 to 3	Parity Enable
W2	----	Not used
W3	Jumper In/Out	Remote/Local Density Select
W4	----	Not used
W5	Jumper In	Adaptive Velocity Control

Also on the Interface PCBA for this tape transport, two terminator resistor packs must be installed at locations G9 and H9.

The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

	DIP Switch Pack				
Switch	SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	ON[2]	OFF	OFF	OFF	through
5	ON[2]			OFF	A-7
6	OFF			OFF	
7	ON[3]			X[4]	
8	ON[5]			OFF	
9	OFF				
10	ON				

[1]See Appendix A, Table A-1.
[2]If OFF, then selecting NRZI selects high-speed 75 ips and jumper W3 should be removed to enable local density select.
[3]ON if odd-numbered tape transport.
[4]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[5]ON if even-numbered tape transport.

B.4 KENNEDY 9400

The Kennedy 9400 tape transport is tri-density (NRZI/PE/GCR), dual-speed 45/75 ips with Pertec interface. It uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard Connector
J100	J1
J200	J2

The tape transport contains a DIP switch pack (S1) with eight DIP switches for option selections. This dip switch pack is located on the upper part of the Pertec Interface PCBA.

VAX/VMS can select between two densities. The settings of the switches in S1 determine the two densities which are available to VMS, as shown in the following table:

Switch	Function	VMS Density Selection PE(800)/ GCR(1600)	NRZI(800)/ GCR(1600)	NRZI(800)/ PE(1600)
1	Formatter Address 0[1]	OFF	OFF	OFF
2	Tape Address 0[1]	OFF	OFF	OFF
3	Tape Address 1[1]	OFF	OFF	OFF
4	Remote Tri-Density	OFF	ON	OFF
5	Interpret Identification	OFF	OFF	ON
6	Interpret Identification	OFF	ON	OFF
7	Variable Speed GCR	OFF	OFF	OFF
8	Variable Speed GCR	OFF	OFF	OFF

[1]Address settings are for Unit 0.

The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch	DIP Switch Pack SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	OFF	OFF	OFF	OFF	through
5	OFF			OFF	A-7
6	ON			OFF	
7	ON[2]			X[3]	
8	ON[4]			OFF	
9	OFF				
10	ON				

[1]See Appendix A, Table A-1.
[2]ON if odd-numbered tape transport.
[3]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[4]ON if even-numbered tape transport.

B.5 STC 1935/1950

The STC 1935 formatter and STC 1950 tape transport are tri-density (NRZI/PE/GCR) units, 125 ips with STC interface and separate formatter. Each model uses the following interface cable connections:

Tape Formatter Connections	Cable Paddleboard Connections
A4	J3 and J4
B4	J5 and J6

The model 1950 requires no jumpers to be positioned and no switches to be set. The model 1935 does have jumpers on the KL PCBA (in slot L2). Jumper connections should be as listed in the following table:

Location	Position	Function
KA67	5 to 10	Enable Retry Correction
KA67	3 to 12	Force Good Parity
KA67	1 to 14	Disable Lost Byte (DO NOT INSTALL)

The tape transport address is selected by plugging the tape transport cables into the formatter as listed in the following table:

Address	Control	Read/Write
0	C5	D5
1	C6	D6
2	C7	D7
3	A7	B7

Terminators on the formatter for the STC 1935 or STC 1950 need not be changed because each tape transport is cabled separately.

The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch	DIP Switch Pack SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	OFF	OFF	OFF	OFF	through
5	OFF			OFF	A-7
6	ON			OFF	
7	ON[2]			X[3]	
8	ON[4]			OFF	
9	ON				
10	ON				

[1]See Appendix A, Table A-1.
[2]ON if odd-numbered tape transport.
[3]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[4]ON if even-numbered tape transport.

B.6 STC 2920

The STC 2920 tape transport is dual-density PE/GCR, 50 ips with STC interface. It uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard PCBA Connector
A4	J3 and J4
B4	J5 and J6

The Interface PCBA on this tape transport has one DIP switch pack at location FA93. Switches in this DIP switch pack must be set as listed in the following table:

SW-1	SW-2	SW-3	SW-4	SW-5	SW-6	Function
OFF	OFF					Address 0
ON	OFF					Address 1
OFF	ON					Address 2
ON	ON					Address 3
					OFF	Horizontal Mounting
					ON	Vertical Mounting

Switches 1 and 2 are used in conjunction. Switches 3, 4 and 5 are not used.

Also on the Interface PCBA of the last tape transport in the daisy chain, two terminator resistor packs must be installed at locations BA45 and BA63.

The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch	DIP Switch Pack SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	OFF	OFF	OFF	OFF	through
5	OFF			OFF	A-7
6	ON			OFF	
7	ON[2]			X[3]	
8	ON[4]			OFF	
9	ON				
10	ON				

[1]See Appendix A, Table A-1.
[2]On if odd-numbered tape transport.
[3]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[4]ON if even-numbered tape transport.

B.7 CIPHER M990

The Cipher M990 tape transport is a tri-density, multiple-speed (70, 100, or 140 ips) cache unit with a Pertec interface. Though the drive itself has three densities (1600 bpi, 3200 bpi, 6250 bpi), the TC7000 only supports two densities while using a Pertec interface (1600 bpi and 6250 bpi). The unit uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard Connector
P1	J1
P2	J2

The tape transport does not have any user-accessible switches or jumpers. All the configuration information is entered via the front panel of the tape transport. The procedure for using the controls and indicators on the front panel can be found in the manual for the tape transport. The configuration should be set to the parameters found in the current Cipher manual.
The switches in five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch	DIP Switch Pack SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	OFF	OFF	OFF	See
2	X[1]	OFF	ON	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	OFF	OFF	OFF	OFF	through
5	OFF			OFF	A-7
6	OFF			OFF	
7	ON[2]			X[3]	
8	ON[4]			OFF	
9	OFF			OFF	
10	ON				

[1]See Appendix A, Table A-1.
[2]ON if odd-numbered tape transport.
[3]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[4]ON if even-numbered tape transport.

B.8 TELEX 9250

The TELEX 9250 tape drive is a digital, vacuum-buffered tape unit with a Pertec interface. It is available in dual-density (9250-200) and tri-density (9250-300) models. VMS may select only two densities with Remote Density Select, 6250 and 1600 bpi. It has a tape speed of 50 ips. It uses the following interface cable connections:

Tape Transport Connector	Cable Paddleboard Connector
I/O 1	J1
I/O 2	J2

The switches in the five DIP switch packs on the TC7000 PCBA must be set to the positions listed in the following table:

Switch		DIP Switch Pack			
	SW1-	SW2-	SW3-	SW4-	SW5-
1	X[1]	ON	OFF	OFF	See
2	X[1]	OFF	OFF	OFF	Tables
3	X[1]	OFF	OFF	OFF	A-5
4	ON[2]	OFF	OFF	OFF	through
5	ON[2]			OFF	A-7
6	OFF			OFF	
7	ON[3]			X[4]	
8	ON[5]			OFF	
9	OFF				
10	ON				

[1]See Appendix A, Table A-1.
[2]If OFF, then selecting NRZI selects high-speed 75 ips and jumper W3 should be removed to enable local density select.
[3]ON if odd-numbered tape transport.
[4]SW4-7 selects VAX-11/780 CPU if ON, or VAX-11/750 CPU if OFF.
[5]ON if even-numbered tape transport.

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